Attansic Technology Corporation.

ATP80

Seven Segment Displayer Controller

Datasheet

Release Date: June. 2001
Revision: 1.0

1. General Description

ATP80 is a Seven Segment Displayer controller. Through the two pins of GPIODA and GPIOCL, ATP80 is able to receive and transmit data from and to SM Bus, and display the data on two Seven Segment Displayers.

It is ideal for the system debugging and status monitoring applications.

2. Features

- Seven Segment Displayer Controller
  - Support up to two Seven Segment Displayers.
- SM Bus Interface
  - Use GPIODA and GPIOCL pins to communicate with system through its SM Bus
- Package
  - SOP 16-Pin

3. Pin Configuration

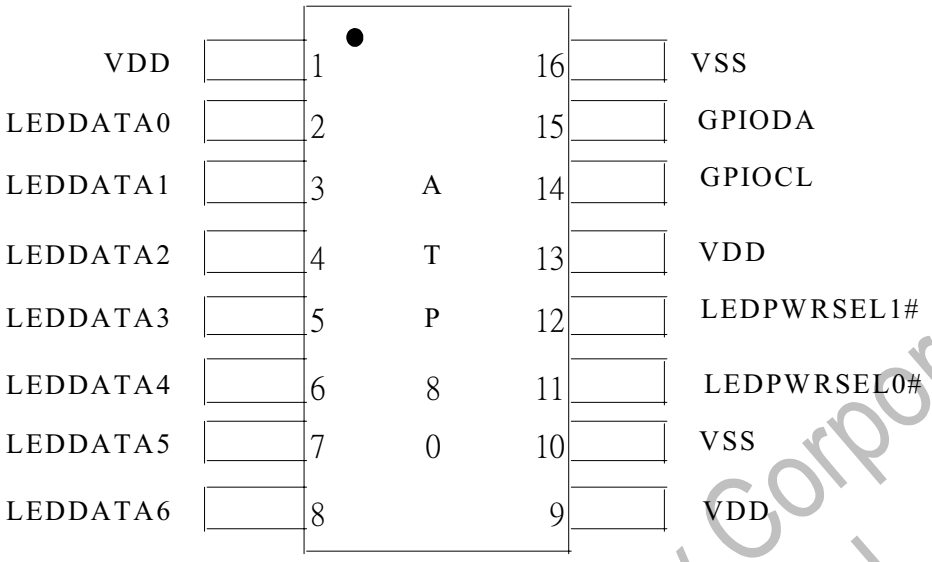
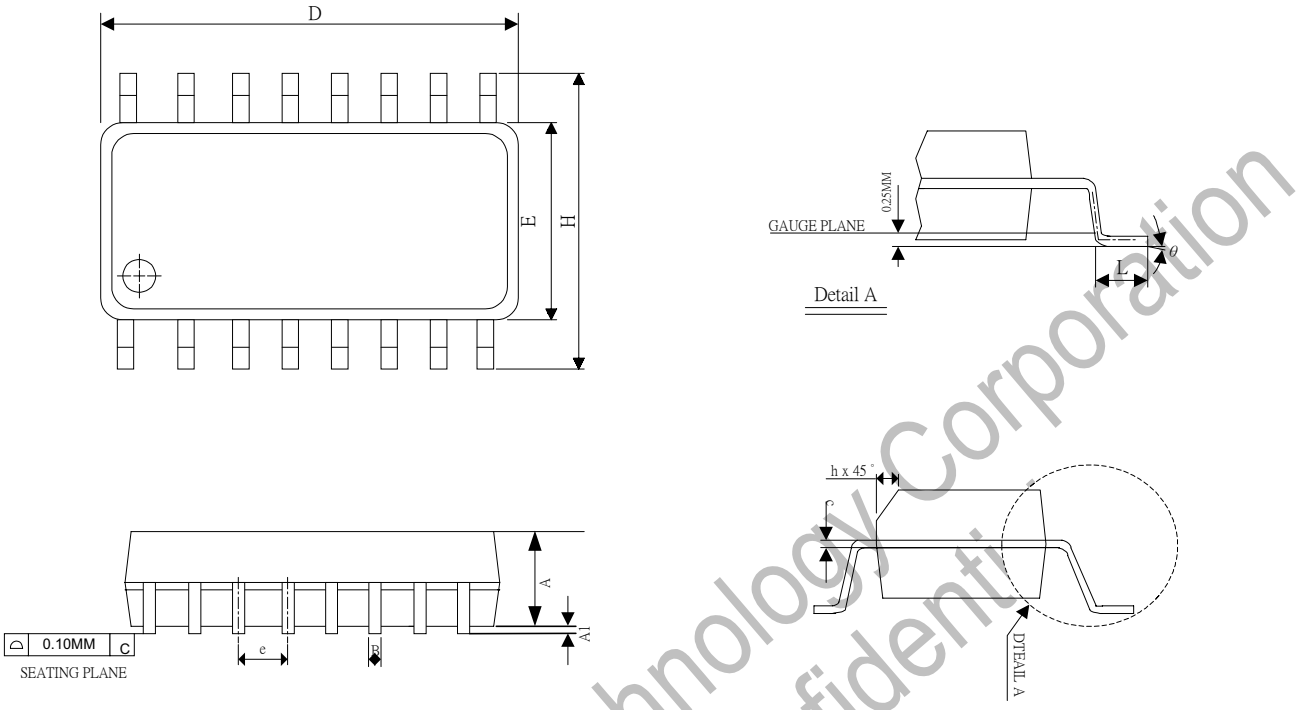


Figure 1. ATP80 Pin Diagram (Top View)

4. Package Information
SOP16pin Outline Dimension



Symbol	Dimension in mm		Dimension in inch	
	Min	Max	Min	Max
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
e	1.27BSC		0.050BSC	
D	9.80	10.00	0.3859	0.3937
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
θ	0^0	8^0	0^0	8^0
JEDEC	MS-012(AC)			

*NOTES: DIMENSION “D” DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

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