



VIA Labs, Inc.

VL150 Electronic Marker for USB Type-C Passive Cables



VIA Labs, Inc.

## Data Sheet

VL150  
E-Marker for USB Type-C Cables

December 5<sup>th</sup>, 2014  
Revision 0.60



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### Revision History

Rev	Date	Initial	Note
0.60	12/5/2014	TS	Preliminary Release

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### VL150 System Overview

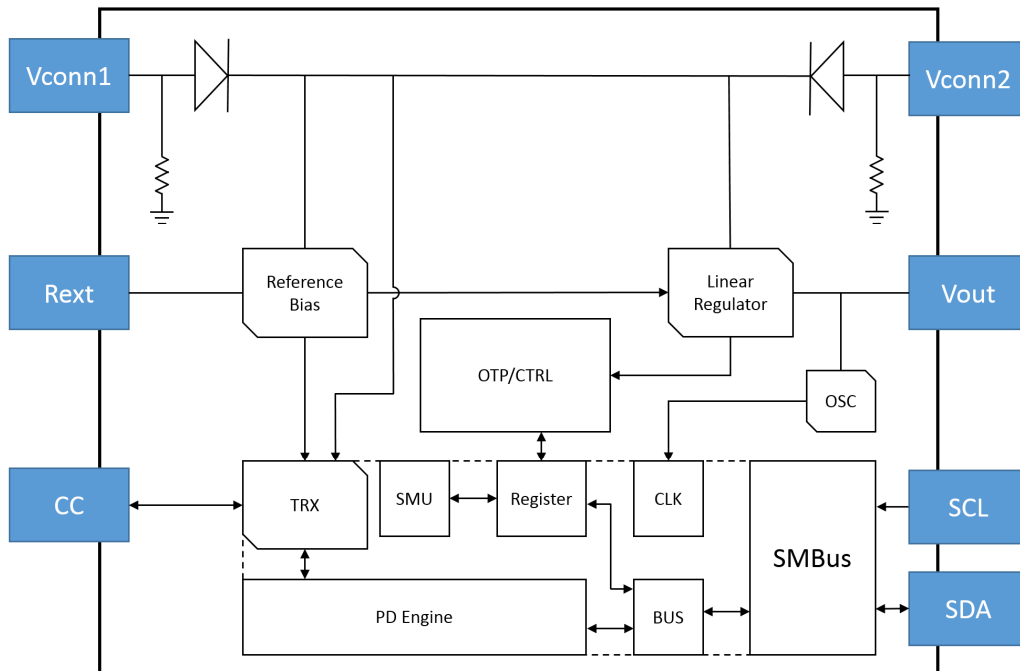


Figure 1 – VL150 Block Diagram

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## Product Features

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### VL150

Electronic Marker for USB Type-C Passive Cables

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#### PD 2.0 Compliant

- Compliant to USB Power Delivery 2.0 Specification
- SOP' Endpoint
- Supports Programming over CC Line using Structured Vendor Defined Messages

#### Sideband Signal Support

- Supports SMBus for Programming and Debugging

#### Easy Manufacturability

- DFN-10 3x3mm features 0.5mm pin pitch for easy manufacturing and can use standard PCB
- VL150 has a default profile prior to programming
- OTP Programming Support over CC or SMBus
- Extremely Low BOM Cost: Diodes, Ra are all integrated On-Die

#### OTP Memory Onboard

- Supports One-Time Writable memory to store Cable VDO, Certificatin Status VDO, Product VDO, etc.
- OTP features write-protection support so finished cables cannot be modified

#### Applications

- Passive USB Type-C Cables such as Full-Featured C-to-C cables.
- This IC is not intended for use in combo PD 1.0 and PD 2.0 applications

#### Platform and Operating System Support

- General support across all major OS and platforms that offer USB such as PC, MAC, Linux, etc.
- FW Update over USB
- USB hub function is dependent upon the USB Host Controller
- No proprietary driver needed, even for Battery Charging Function

#### Misc

- Optimized for Low Power consumption

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Pinout

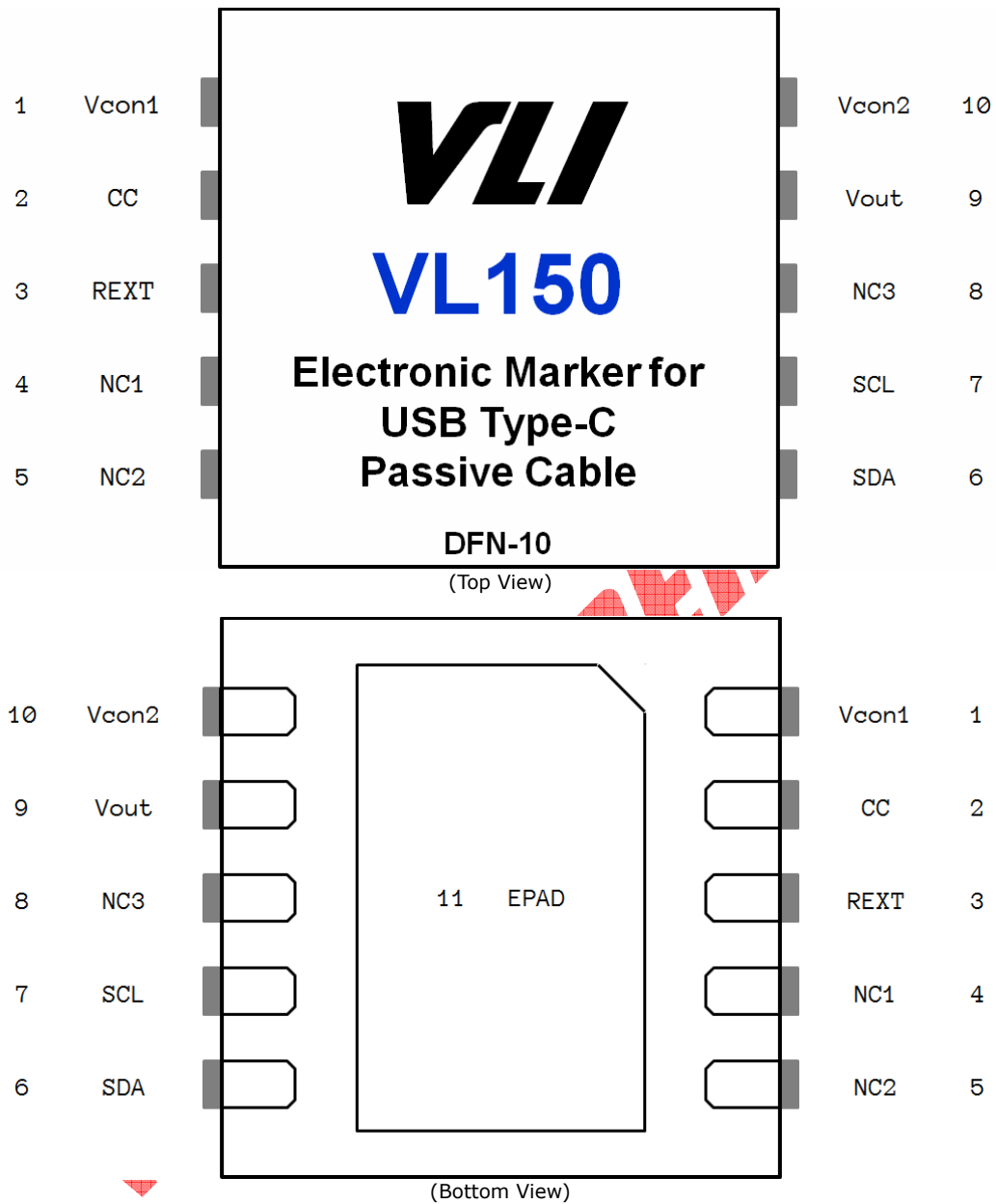


Figure 2 – VL150 Pin Diagram (DFN-10)



## Pin List

Pin	Pin Name	Pin	Pin Name
1	Vcon1	6	SDA
2	CC	7	SCL
3	REXT	8	NC3
4	NC1	9	Vout
5	NC2	10	Vcon2
		11	EPAD

## Pin Descriptions

## Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

## Type-C Interface

Pin Name	Pin #	I/O	Signal Description
Vcon1	1	PWR	Vconn Power (Near Side)
CC	2	I/O	CC communication line
Vcon2	10	PWR	Vconn Power (Far Side)

## Sideband &amp; Miscellaneous

Pin Name	Pin #	I/O	Signal Description
SCL	24	I	SMBus Clock (Open Drain)
SDA	23	I/O	SMBus Data (Open Drain)
NC1	27		Not Connected (Float)
NC2	26		Not Connected (Float)
NC3	25		Not Connected (Float)

## Power &amp; Ground

Pin Name	Pin #	I/O	Signal Description
REXT	3	O	External Reference Resistor (120K 1%)
Vout	9	PWR	Connect to 1uF X5R Capacitor
EPAD	11	GND	Exposed Pad; System Ground



## Electrical Specification

**Absolute Maximum Rating**

Symbol	Parameter	Min	Max	Unit	Note
T <sub>STG</sub>	Storage Temperature	-55	125	°C	—
V <sub>CON1/2</sub>	Vconn	-0.5	7	V	—
V <sub>ESD</sub>	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ <sub>jc</sub>	Thermal resistance between junction and case	● TBD		°C/W	2L & 4L PCB definitions follow JESD51-7
P <sub>D</sub>	Max Power Dissipation	—	TBD	W	

Note: Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T<sub>a</sub> is the concerned ambient temperature, and

$$\theta_{ca} = \theta_{ja} - \theta_{jc}$$

$$T_j = \theta_{ja} * P_D + T_a$$

$$T_c = \theta_{ca} * P_D + T_a$$

**Operating Conditions**

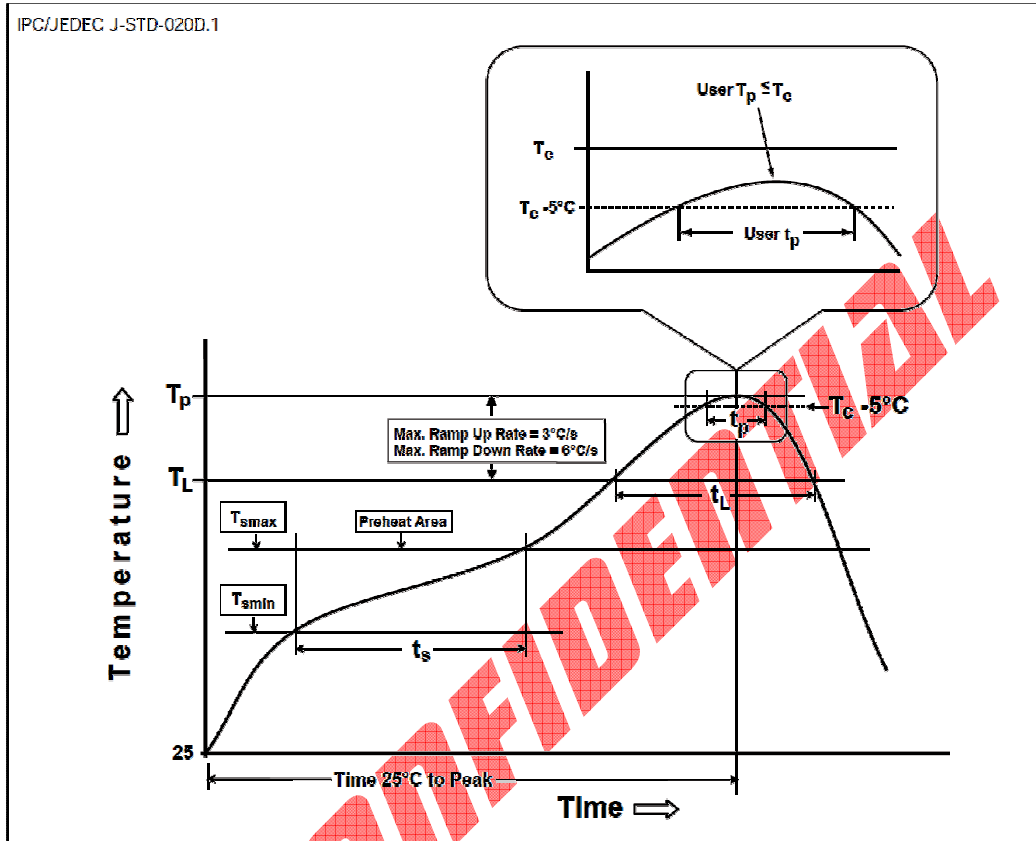
Symbol	Parameter	Min	Max	Unit	Note
T <sub>A</sub>	Ambient Temperature	-25	85	°C	TBD
T <sub>j</sub>	Junction Temperature	0	125	°C	—
V <sub>CON1/2</sub>	Vconn	4	5.5	V	—

Power Consumption:

Operation: <70mW

Suspend: <7.5mA

## General Reflow Profile Guidelines.



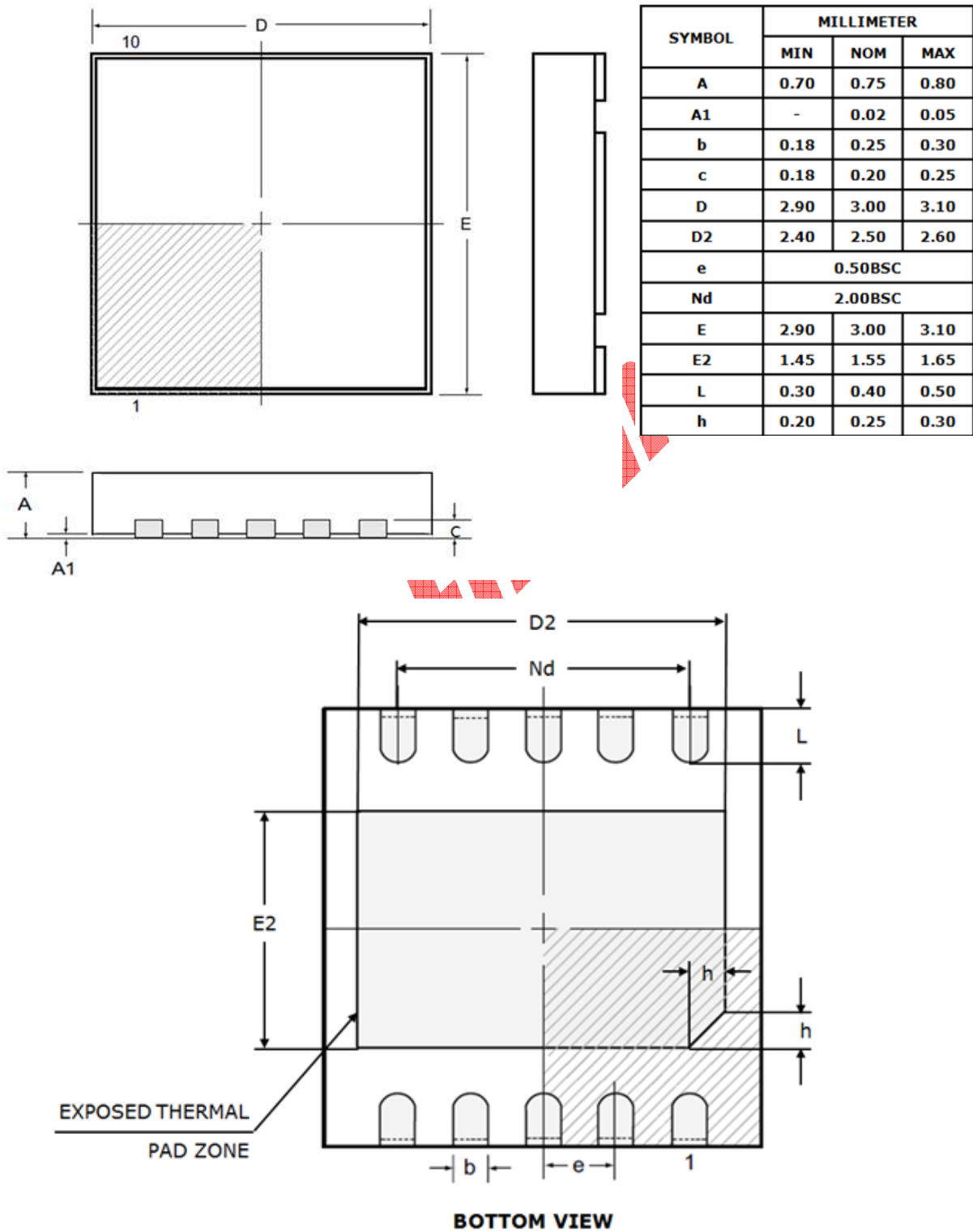
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat/Soak</b>		
Temperature Min ( $T_{smin}$ )	100 °C	150 °C
Temperature Max ( $T_{smax}$ )	150 °C	200 °C
Time ( $t_s$ ) from ( $T_{smin}$ ) to ( $T_{smax}$ )	60-120 seconds	60-120 seconds
Ramp-up rate ( $T_L$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time ( $t_L$ ) maintained above $T_L$	60-150 seconds	60-150 seconds
Peak package body temperature ( $T_p$ )	225 °C	250 °C
Classification temperature ( $T_c$ )	230 °C	255 °C
Time ( $t_p$ )* within 5 °C of the specified classification temperature ( $T_c$ )	20* seconds	30* seconds
Ramp-down rate ( $T_p$ to $T_L$ )	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug).

Figure 6 – Reflow



### Package Mechanical Specifications (DFN-10)



Package Top Side Marking & Ordering Information



L150: Product Name  
 ABC: Wafer Lot Serial Number  
 Y: Year Code  
 WW: Week Number

Ordering Information	Description	Package Type
VL150-D1	VL150 Tape and Reel (3K)	DFN10 3x3 mm



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