A Reconfigurable Computing System Based on a Cache-Coherent Fabric

Presenter: Neal Oliver
Intel Corporation

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Authors- Neal Oliver, Rahul R Sharma, Stephen Chang, Bhushan Chitlur, Elkin Garcia, Joseph Grecco, Aaron Grier, Nelson Ijih, Yaping Liu, Pratik Marolia, Henry Mitchel, Suchit Subhaschandra, Arthur Sheiman, Tim Whisonant, and Prabhat Gupta

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Topics

- Motivations for this work
- Usage Models
- Overview of Intel QuickPath Interconnect (QPI)
- Platform Architecture
- Hardware Architecture
- Programming Model
- Simulation
- Future Work

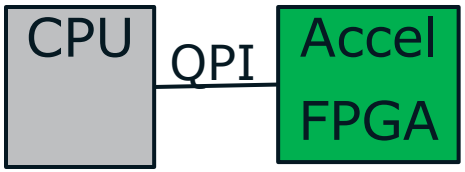
Motivation for this work

- Keep innovation on Intel platforms
- High-throughput, low-latency attachment to server
- Cache-coherent memory
  - Enlarge memory space for FPGA platform
  - Enable additional programming paradigms
- Drive requirements for future fabrics
- Platform for simulation/emulation

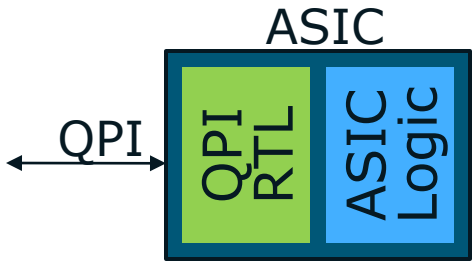
Usage Models

Intel QuickAssist Accelerator Platform (QAP)

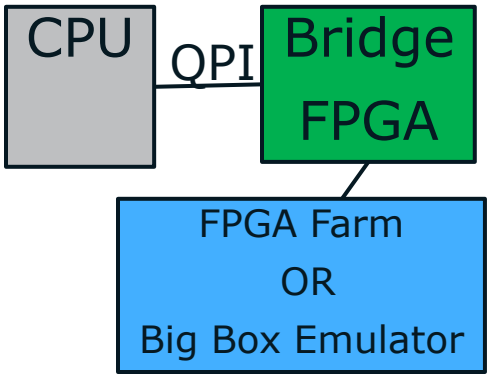
Accelerators
- Algorithmic accelerators
- e.g. Seismic imaging, genomics, computational finance



ASIC Prototyping
- Significantly reduces risk for ASICs connecting to QPI
- e.g. QPI attached ASICs for telecom, node controllers



HW/SW Co-Emulation Platforms
- Enables development of high performance emulation platforms
- Pre-Si SW development



Intel QuickPath Interconnect (QPI)

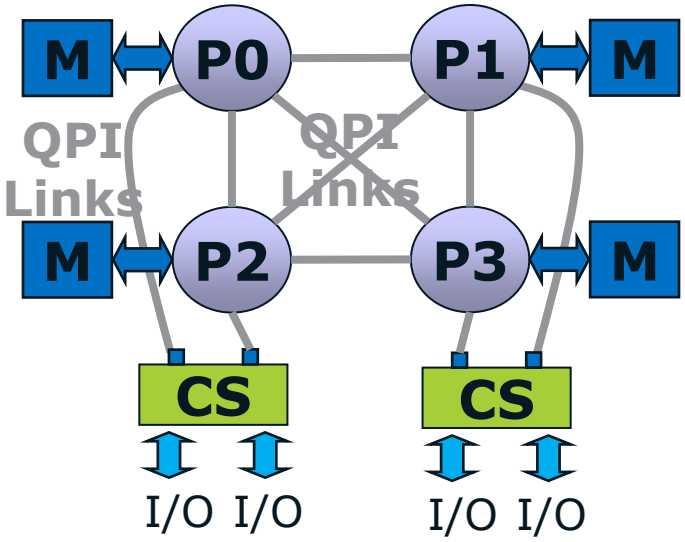
QPI: A low latency, point-to-point coherent system interconnect.

QPI Caching Agent (CA) – cache devices

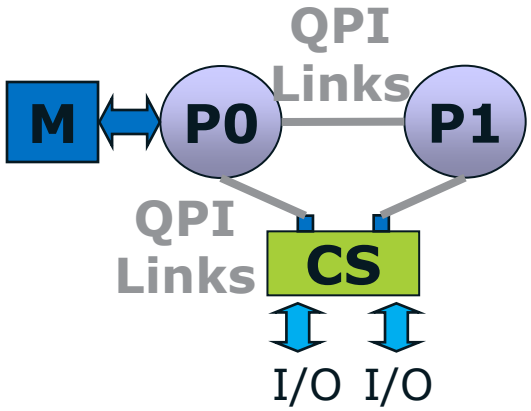
QPI Home Agent (HA) – DDR memory controller

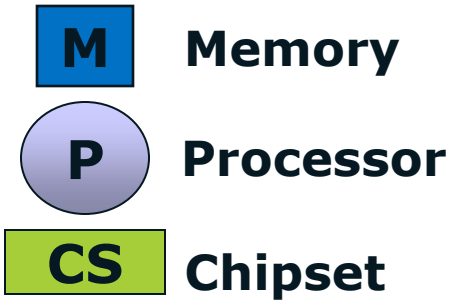
Latest Intel platforms have IO integrated into CPU (not shown)

Four Socket Platform



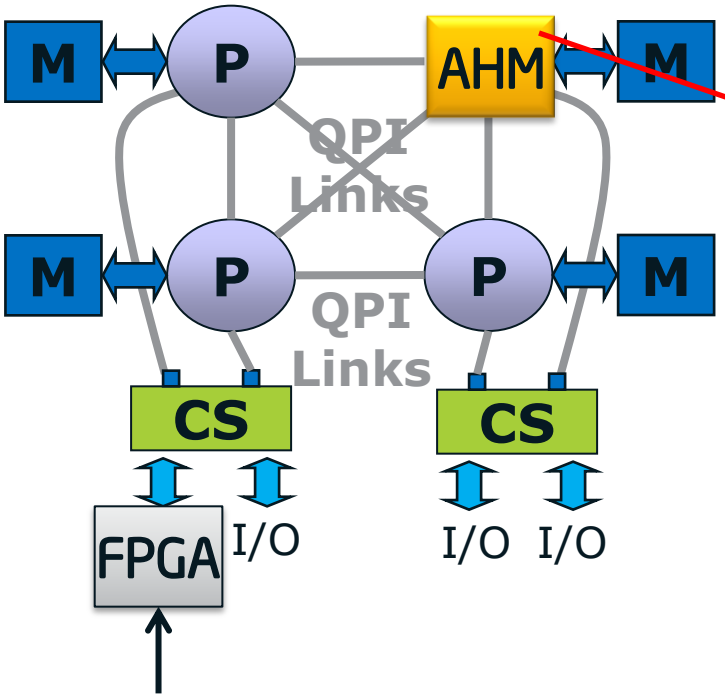
Two Socket Platform





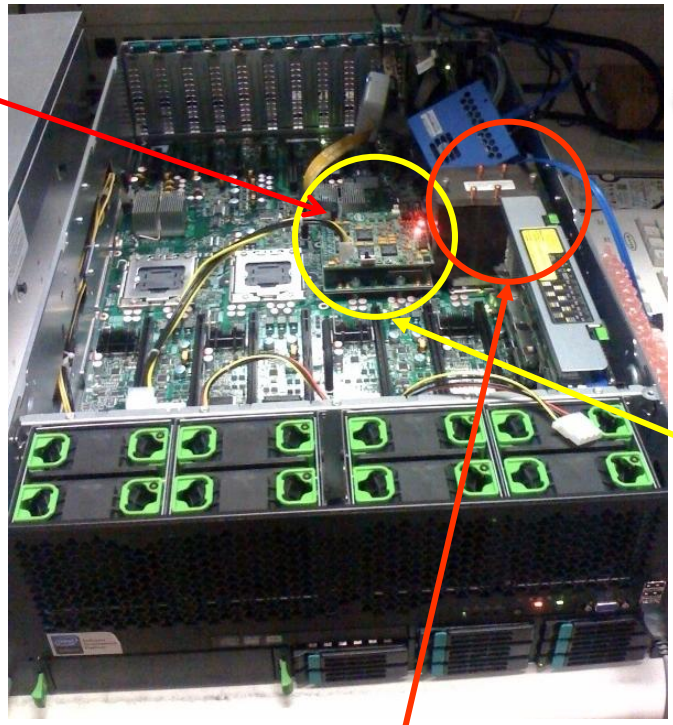
QPI-attached Accelerator Hardware Module (AHM)

Substitution of AHM for CPU



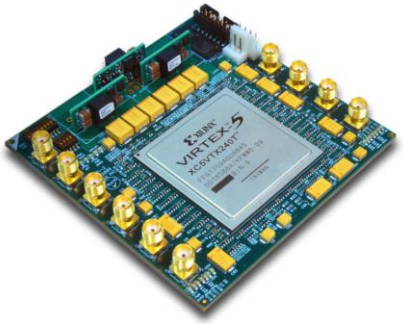
PCIe attached FPGA

AHM installed in Server



Intel® Xeon processor 7000 series

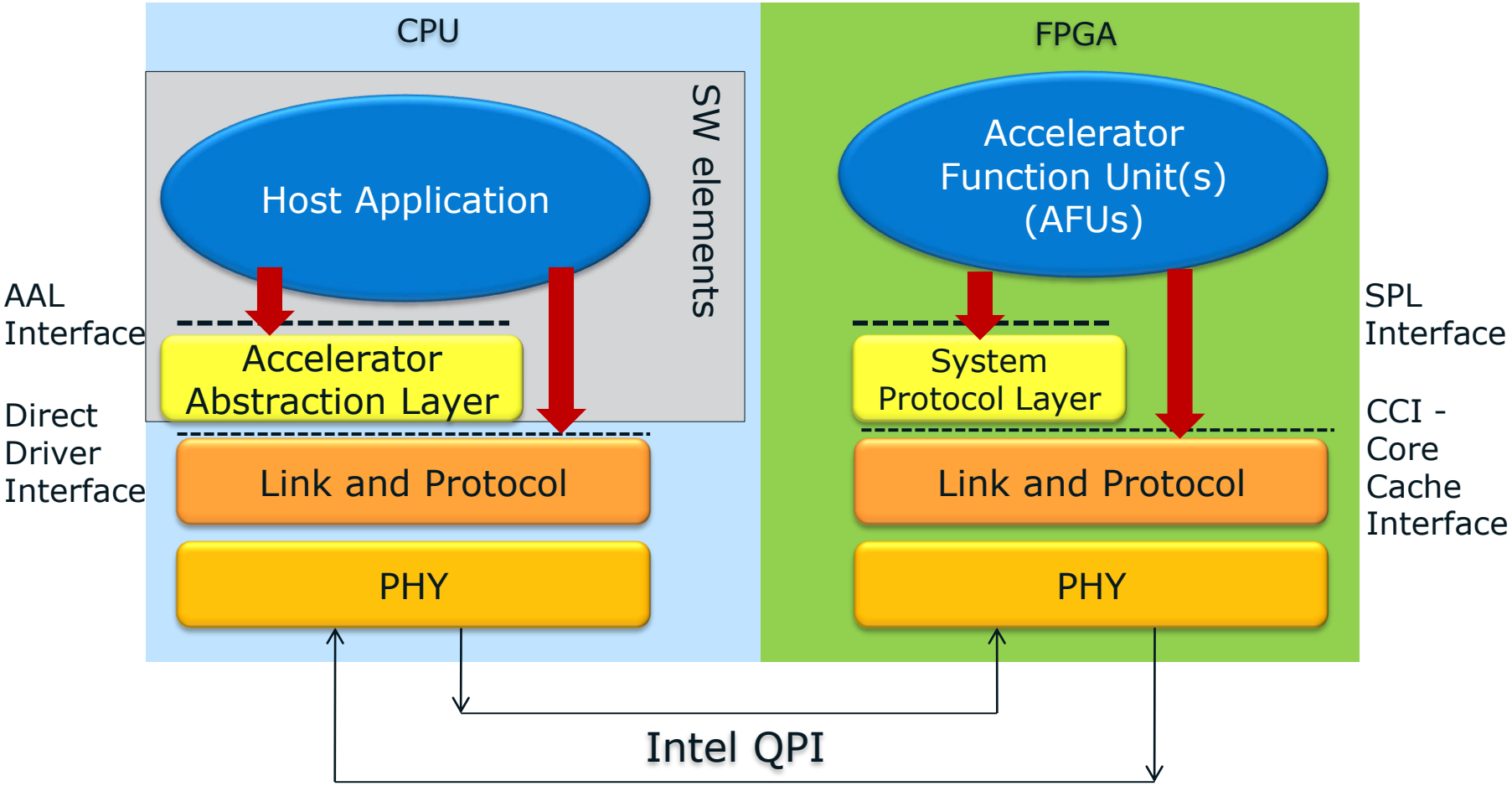
Accelerator Hardware Module (AHM)



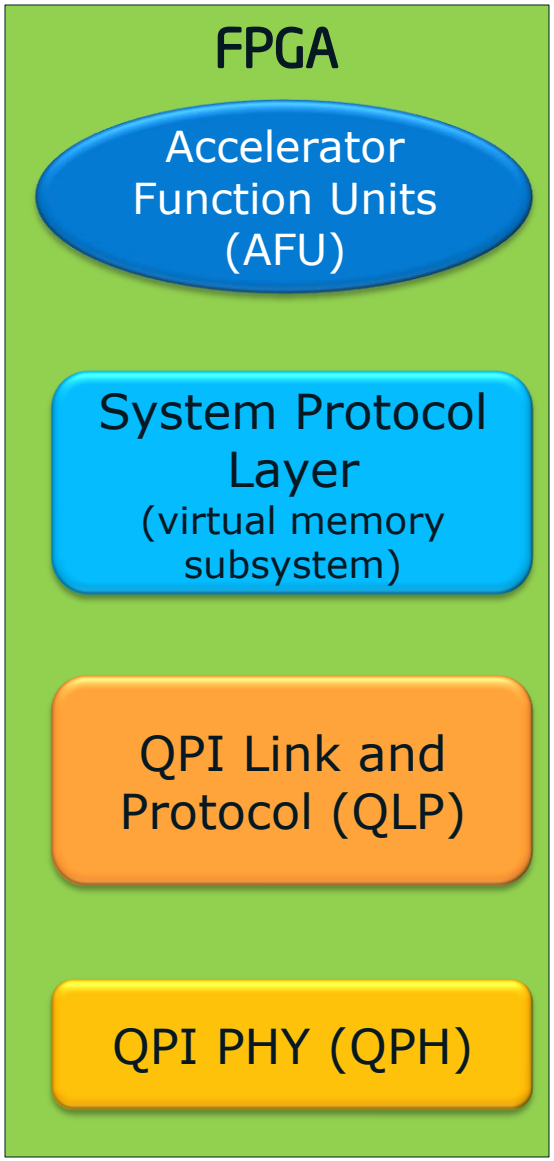
Xilinx Virtex 6 Module

Altera Stratix IV Module

Platform Architecture



QPI HW stack



- Application-specific hardware module, user algorithm to be accelerated.
- Can connect to SPL or CCI interface

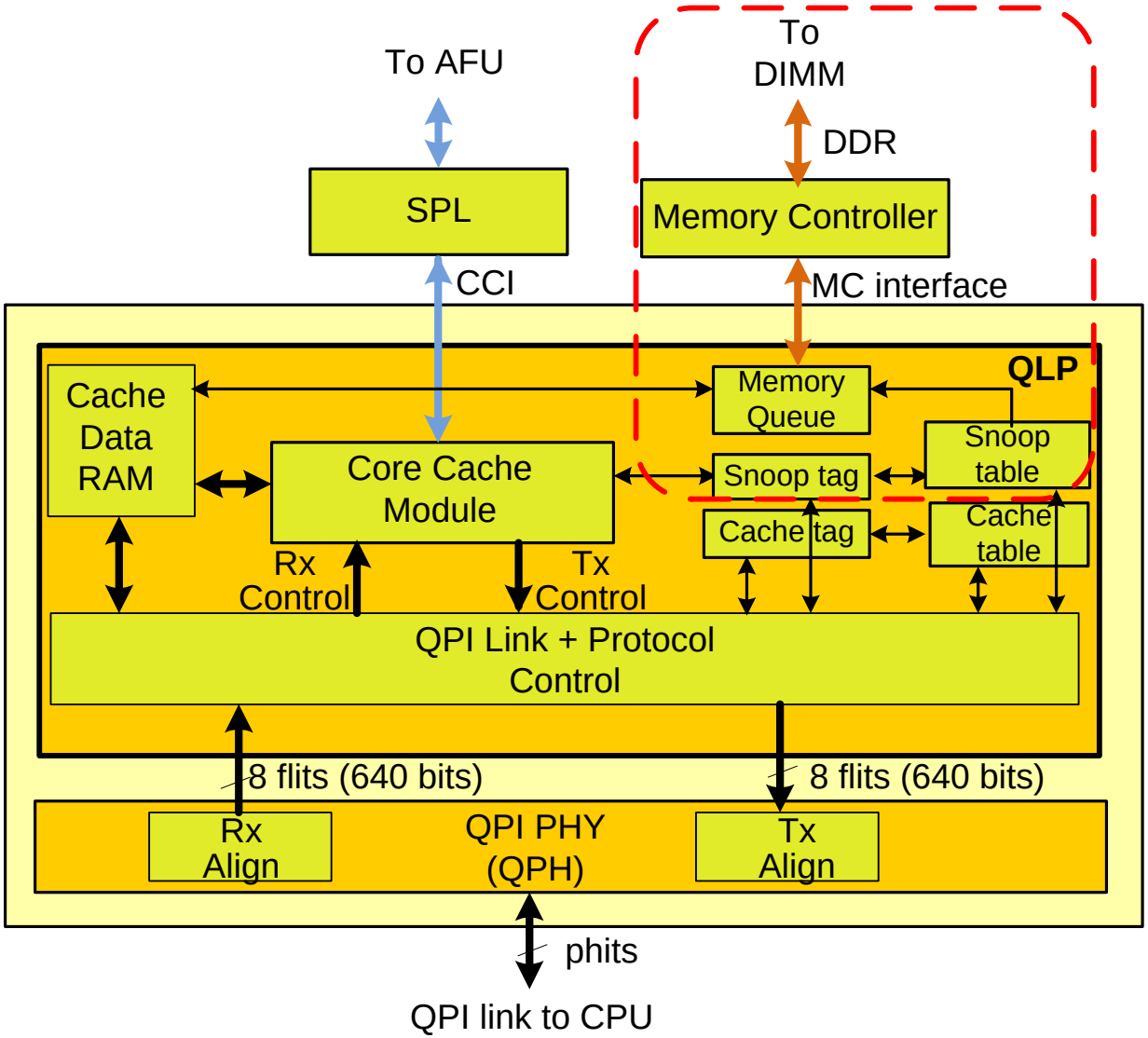
- Implements virtual to physical address translation
- Handles all cache line reordering in blocks of data
- DMA engine
- Memory management and protection

- QPI Caching (cache) and Home Agent (memory controller) implemented
- 64KB to 256KB set-associative cache
- Manages coherency of FPGA attached DDR memory

- FPGA high speed IO operating at 4.8 to 6.4 GT/sec
- Full width : 20 data lanes per direction

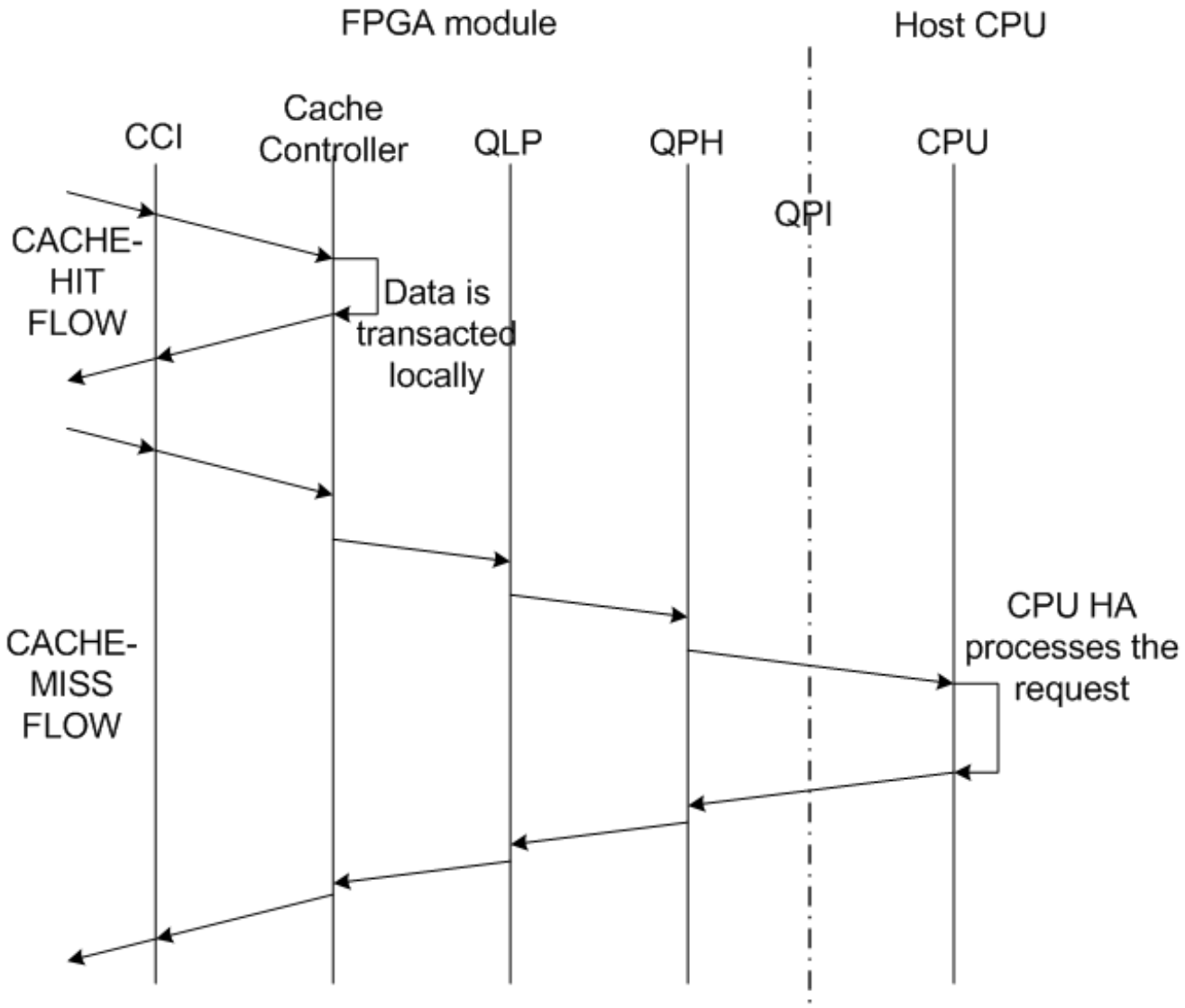
QPI Home+Cache Agent Architecture

- Modular: CA, HA, CA+HA
- Interfaces:
CCI- hides complexity of underlying coherent fabric.
MC (optional) – provides interface to memory controller.
- QPH electrical uses existing FPGA IOs
- QLP designed using soft logic, tightly integrated, highly parallel.
- Programmable cache/snoop tables



Cache Hit/Miss protocol flow

- Cache hits are an order of magnitude faster.
- Prefetch striding patterns to improve cache hit rate



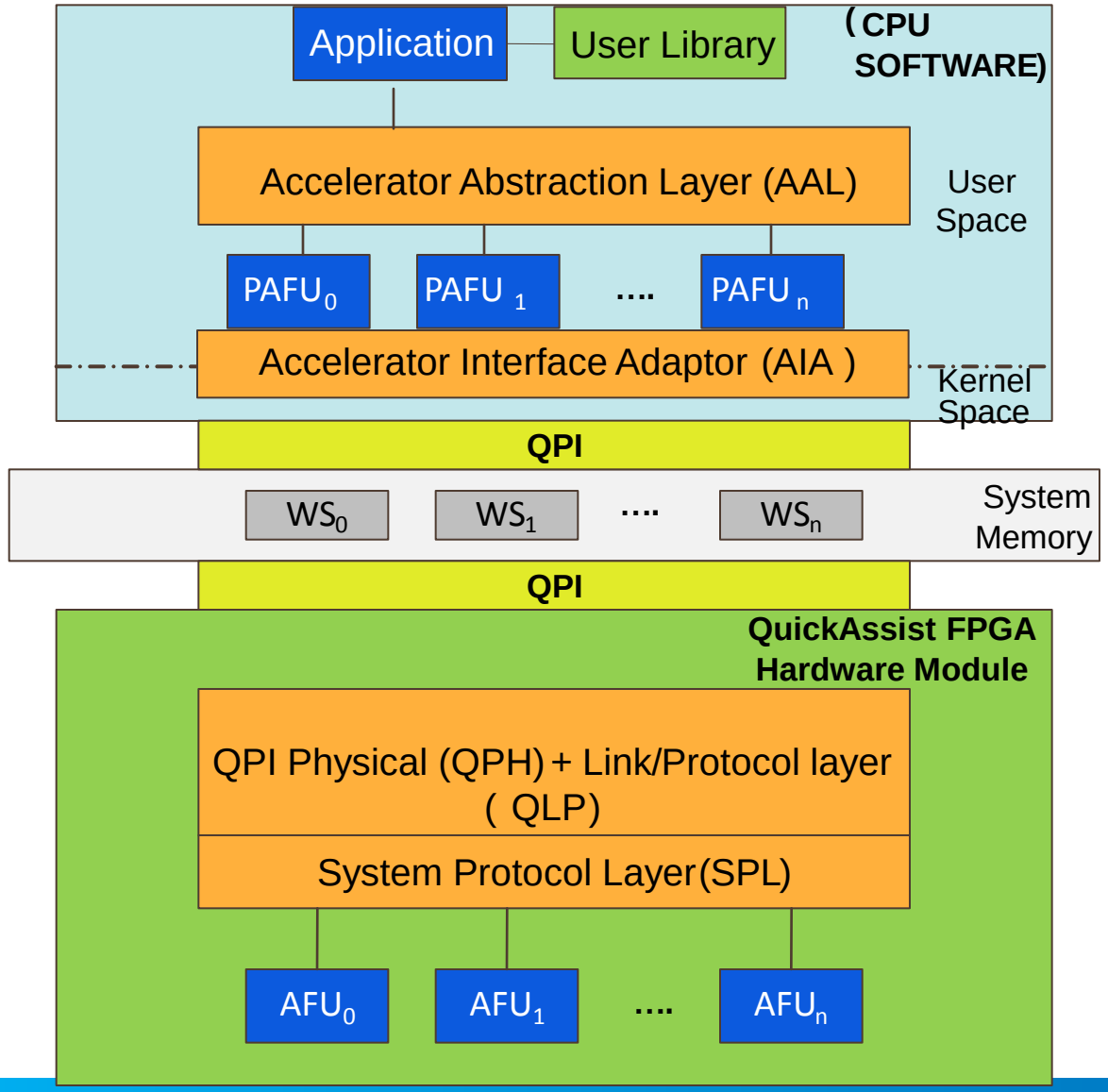
Programming Model

AAL functions:

- Allocate shared workspaces WS_i and pin in system memory
- Support both physical and virtual memory access
- Allocate and manage AFUs for application (via "proxy AFU" ($PAFU_i$) abstraction)
- Provide remote procedure call (RFP) abstraction of AFU to application

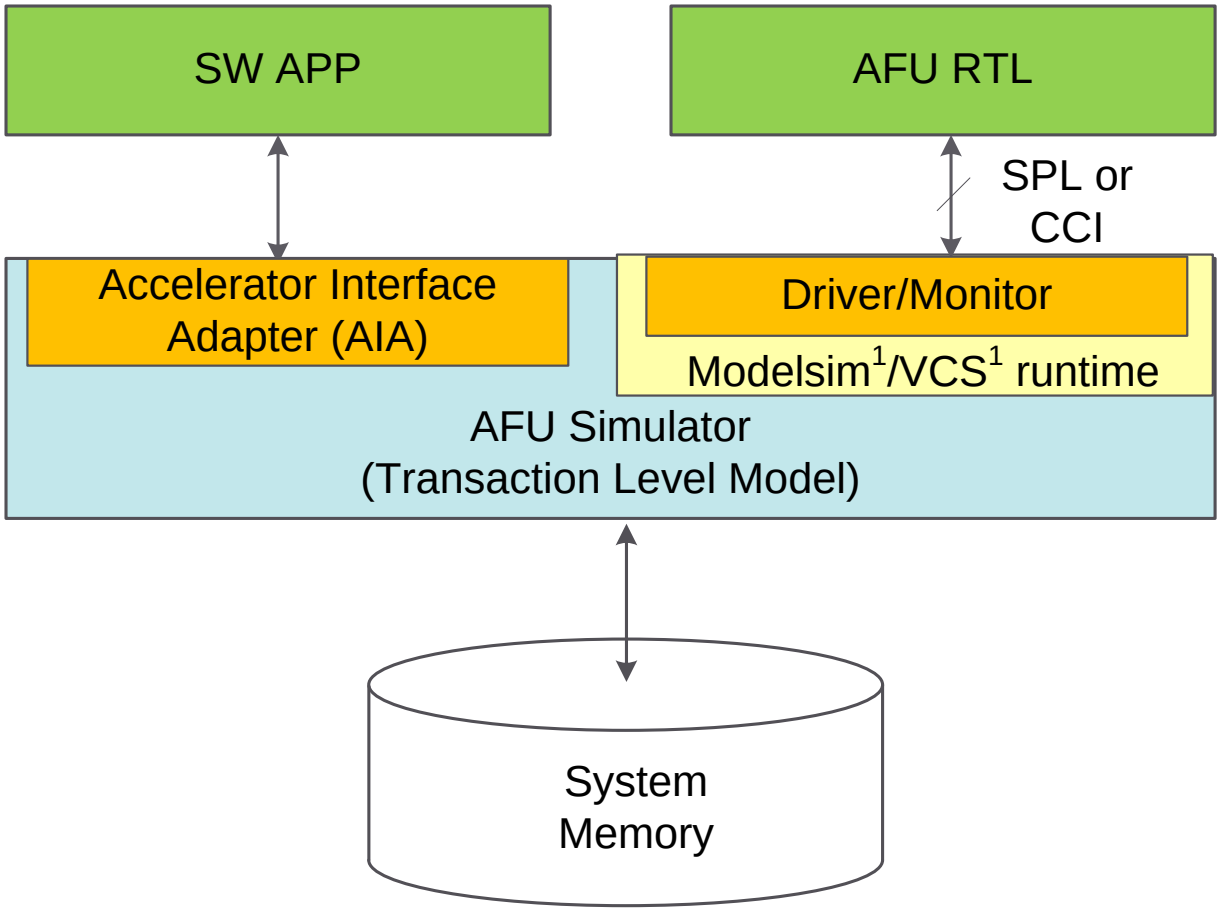
Proxy AFU:

- Provide abstraction of AFU to application
- Enables staged development of AFU algorithms



AFU Simulation Environment (ASE)

- AFU HW-SW co-design environment.
- Models platform behavior.
- Design and validate the SW against the AFU RTL in the simulator environment.
- Faster simulation.
- Ease of debug.



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Future Work

- Research and pathfinding on other accelerator architectures
- Programming language/compiler development
- Benchmarking and performance characterization

Thank You

Contact – p.k.gupta@intel.com
neal.oliver@intel.com