DDR5: Fifth-generation of DDR Memory Module

Anil Pandey

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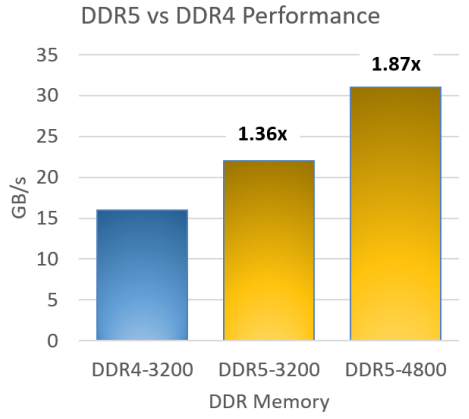
The latest buzz on next-generation memory is DDR5, the successor of DDR4. DDR5 is latest and next-generation (fifth-generation) of double-data-rate (DDR) random-access memory (RAM) memory family. The key features driving future memories are speed, memory density, lower operating voltage, and faster access. DDR5 supports memory density from 8Gb to 64Gb along with a wide range of data rates from 3200 MT/s to 6400 MT/s.

DDR5 is mainly driven by the need for more bandwidth while previous generations focused on reducing power consumption and were driven by applications such as mobile and data center. It will provide double the bandwidth over DDR4, along with delivering improved channel efficiency but the primary feature of DDR5 SDRAM is the capacity of chips. DDR5 is denser and enables greater quantities of memory in similar form factors to DDR4. The speed that DDR5 is 16x faster than the first-ever SDRAM.

Memory Type	Bandwidth	Data rates (MT/s)	Bus Clock (MHz)	DIMM pins	Voltage (V)	Release Year	Prefetch	Termination/ODT	Bank Group	Chip Densities
SDR	1.6 GB/s	100-166	100-166	168	3.3	1993	1n	Ohms on board	0	128MB-512 MB
DDR1	3.2 GB/s	266-400	133-200	184	2.5/2.6	2000	2n	Ohms on board	0	128MB-1GB
DDR2	8.5 GB/s	533-800	266-400	240	1.8	2003	4n	ODT added	0	128 MB-4 GB
DDR3	17 GB/s	1066-1600	533-800	240	1.35/1.5	2007	8n	Nominal dynamic modes	0	512 Mb-8GB
DDR4	25.6 GB/s	2133-3200	1066-1600	380	1.2	2014	8n	Park modes	4	2 GB-16 GB
DDR5	**32GB/s**	**3200-6400**		**380**	**1.1**	**2019**	**8/16n**	**Nominal Wr/Rd**	**8**	**8 Gb-64 GB**

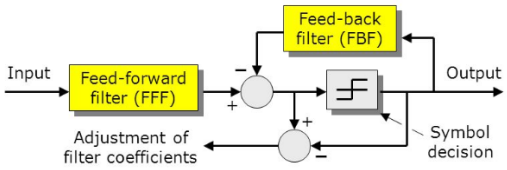
DDR5 Data Rates

At a higher data rate, DDR5-4800, the estimated performance increase becomes 1.87x which is nearly double the bandwidth as compared to DDR4-3200 (*Source: Micron*), with a supply voltage drop to 1.1 V and an allowable fluctuation range of 3% (i.e., at ±0.033V).

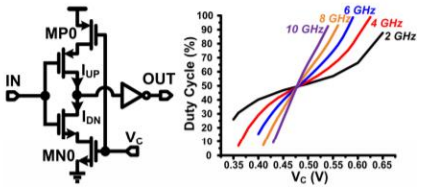


This increase in the I/O switching rate (data rate) is realized without the need for differential signaling at the DQ pins; the DQ bus remains single-ended, pseudo-open drain (POD). There are many new features that enable these higher data rates;

1. DFE- The addition of equalization in the form of a multi-tap decision feedback equalizer (DFE) in the DQ receivers enables high data rate. The DFE moderates the effects of inter-symbol interference (ISI) at the higher rates by opening the data eyes inside the device.



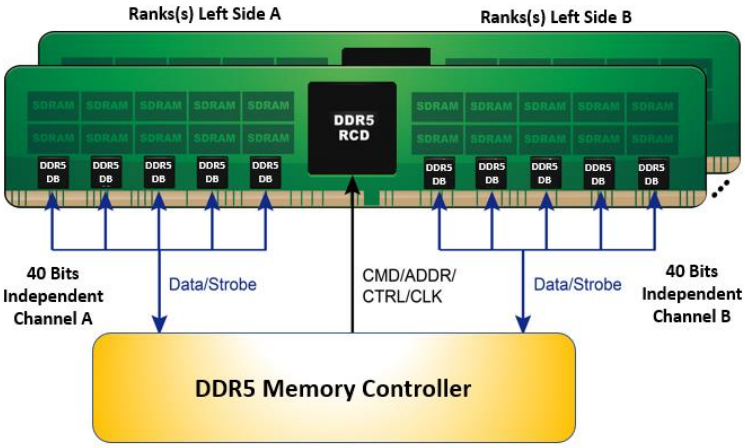
2. DCA - Duty cycle adjuster (DCA) circuit helps to correct the small duty cycle distortions, ultimately optimizing the duty cycles for the DQ and DQS signals received by the controller.



3. Training modes- DDR5 includes a new read preamble training mode, chip select training mode, command and address training mode, and a write leveling training mode.
4. DQS interval oscillator circuit that allows the controller to monitor changes in the DQS clock tree delays caused by shifts in voltage and temperature.
5. Write pattern command – It saves power by not sending the data across the bus.
6. On-die termination (pulled-up VDDQ) will be available for address buses, not just data buses

DDR5 Protocol Features for Improved Performance

High-end DDR5 DIMMs will have their own voltage regulators and PMICs. DDR5 DIMMs comprise two 40-bit (32-bit + ECC) independent channels per module. This allows a single burst to access 64B of data when combined with a new default burst length of 16 (BL16) in the DDR5 component. In DDR5, the channels will have their own 7-bit address and command buses so it will have an improved command bus efficiency. These buses already feature on-die termination to make signals cleaner and to improve stability at high data rates.



JEDEC (an independent semiconductor engineering trade organization and standardization body) still hasn't approved an official specification for DDR5, and they are very strict about not allowing anyone to claim DDR5 compatibility until the standard is complete. Though, there is official standard for Low-Power DDR5 (LPDDR5), which doubles the base speed over LPDDR4 from 3,200 MT/s (mega transfers per second) to 6,400 MT/s. Major memory manufacturers, SK Hynix (DDR5 in desktop and laptop PCs) and Samsung (mobile devices) both announced in early 2019 that there would be DDR5-based products out before the end of the year. The news of DDR5 has naturally sparked huge amounts of interest from both enthusiasts and professionals but at this moment there are several questions that currently surround the latest DDR5 memory.