4.1.6 Definitions of the EE1004-v 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 Kbit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications

1. SCOPE

This standard defines the specifications of interface parameters, signaling protocols, and features for Serial Presence Detect (SPD) EEPROM (EE) and Temperature Sensor (TS) as used for memory module applications. The designations EE1004-v and TSE2004av refer to the families of devices specified by this document.

The purpose is to provide a standard for the EE1004-v and TSE2004av devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

A single specification document for both families of devices is written to establish and maintain the commonality of these devices and promote the interchangeability of devices in target applications that may require the EE and TS for some uses and EE only for other uses. When a portion of this specification refers to both classes of devices, the abbreviation EE/TSE is used.

NOTE: The designations EE1004-v and TSE2004av refer to the part of the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2. DEVICE STANDARD

2.1. Description

The EE1004-v is a 512-byte EEPROM device. The TSE2004av is a combination 512-byte EEPROM and Temperature Sensor device. The EE/TSE devices are designed to operate in one of two voltage ranges, 1.7-3.6 V or 2.2-3.6 V. All EE/TSE 2.2-3.6 V nominal devices shall operate the I^2C Bus up to 1 MHz maximum (Fast Mode+). Operation to 100 KHz compliant with SMBus 2.0 operation. EE/TSE devices are intended to interface to I^2C Buses which have multiple devices on a shared bus, and must be uniquely addressed on this bus. A substantial reduction in supply current may be achieved using the software programmed shutdown mode.

2.2. Common Features summary:

EE1004-v Variations						
Base part number					**v**	Single Supply Voltage
EE1004					1	1.7 to 3.6 V
					2	2.2 to 3.6 V
TSE2004av Variations						
Base part number		**a**	Sensor Accuracy		**v**	Single Supply Voltage
TSE2004		B	0.5 °C typ from 75-95 °C		1	1.7 to 3.6 V
			1.0 °C typ from 40-125 °C		2	2.2 to 3.6 V
			2.0 °C typ from -20-125 °C			
Examples: 1. EE1004-1 is a 512-byte SPD with a single supply voltage range from 1.7 to 3.6 V. 2. TSE2004B2 is a 512-byte SPD with Thermal Sensor having 0.5 °C typical accuracy from 75-95 °C and a single supply voltage range from 2.2 to 3.6 V.						

- Low operating current:
  < 100 uA maximum with EE in Standby and TS in Shutdown mode
  ~1 mA typical with EE in Standby mode and TS active
  ~2 mA typical with TS and EE enabled at 3.3 V input
- Two Wire I^2C Bus Serial Interface
- Up to 100 kHz Transfer Rate below 2.2 V compliant with SMBus 2.0
- Up to 1 MHz Transfer Rate (Fast Mode+ I^2C Bus compliant) at or above 2.2 V
- Package: Thermally Enhanced PSON-8 standard for all JEDEC module applications

EE Features summary(EE/TSE):

- Individual Reversible Software Data Protection for all four 128 Byte Blocks
- Byte and Page (up to 16 Bytes) Write Operation
- Random and Sequential Read modes
- Self-Timed Write Cycle
- Automatic Address Incrementing

TS Features summary (TSE2004av only):

- Typical accuracy of 0.5 °C accuracy for the active range from 75 ~ 95 °C
- Typical accuracy of 1.0 °C for other monitor ranges from 40 ~ 125 °C
- Ambient temperature (TA) sense through an operating range of -20 to +125 °C
- Temperature sample rate minimum of 8 samples/s
- Selectable 0, 1.5 °C, 3 °C, 6 °C Hysteresis on set point

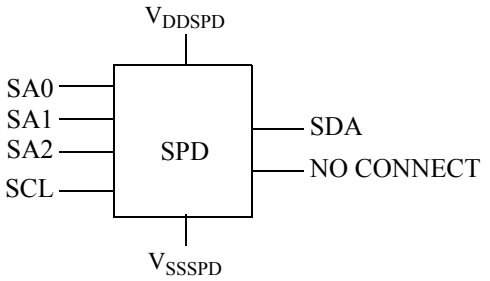
The EE/TSE devices include a 4 Kbit serial EEPROM organized as two pages of 256 bytes each, or 512 bytes of total memory. Each page is comprised of two 128 byte blocks. The devices are able to selectively lock the data in any or all of the four 128-byte blocks. Designed specifically for use in DRAM DIMMs (Dual Inline Memory Modules) with Serial Presence Detect, all the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in one or more of the blocks of memory.

The EE/TSE devices are protocol compatible with previous generation 2 Kbit devices such as the EE1002(A) and TSE2002av. The page selection method allows commands used with legacy devices such as EE1002(A) and TSE2002av to be applied to the lower or upper pages of the EE/TSE. In this way, the EE/TSE may be used in legacy applications without software changes. Minor exceptions to this compatibility, such as elimination of the Permanent Write Protect feature, are documented.

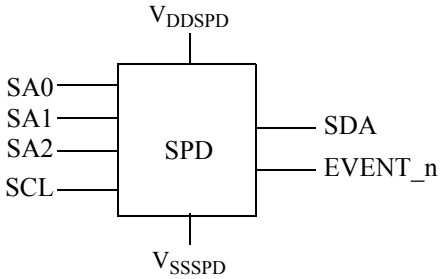
Individually locking a 128-byte block of the EE may be accomplished using a software write protection mechanism in conjunction with a high input voltage V_{HV} on input SA0. By sending the device a specific I^2C Bus sequence, each block may be protected from writes until write protection is electrically reversed using a separate I^2C Bus sequence which also requires V_{HV} on input SA0. Write protection for all four blocks is cleared simultaneously, and write protection may be re-asserted after being cleared.

The Thermal Sensor (TS) section of the TSE2004av continuously monitors the temperature and updates the temperature data a minimum of eight times per second. Temperature data is latched internally by the device and may be read by software from the bus host at any time.

Internal registers are used to configure both the TS performance and response to over-temperature conditions. The device contains programmable high, low, and critical temperature limits. Finally, the device EVENT_n pin can be configured as active high or active low and can be configured to operate as an interrupt or as a comparator output.



EE1004-v Device Diagram



TSE2004av Device Diagram

Figure 1 — Device Diagrams

2.3. Device Interface

The EE/TSE behaves as a slave device in the I^2C Bus protocol, with all operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R/W_n bit (as described in Table 3 on page 7), terminated by an acknowledge bit. EE/TSE family devices shall not initiate clock stretching, which is an optional I^2C Bus feature.

In accordance with the I^2C Bus definition, the EE/TSE devices use three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and a 3-bit Select Address to generate an I^2C Bus Slave Address. The EE memory may be accessed using a DTIC of (1010), and to perform the SWPn, RSPn, or CSWP operations, a DTIC of (0110) is required. The TS registers of the TSE2004av are accessed using a DTIC of (0011).

EE and TS portions of TSE devices are designed to operate in parallel. Accesses to each portion of the device may be interleaved as long as the command protocol is followed.

2.3.1. EE/TSE Serial Address Selection

Inputs SA0, SA1, and SA2 inputs are directly combined with the DTIC and the EE page address bit to qualify I^2C Bus addresses. Each of the SA pins is tied to V_{DDSPD} or V_{SSSPD} and the Logical Serial Address (LSA) is equal to the code on the Serial Address pins.

Table 1 — I^2C Bus Addressing Modes

Logical Serial Address (LSA)	SA2	SA1	SA0
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0
101	1	0	1
110	1	1	0
111	1	1	1
Note 1: 0 = V_{SSSPD}, 1 = V_{DDSPD}			

2.4. Interface Protocol

When writing data to the memory, the EE/TSE inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ.

Violations of the command protocol result in unpredictable operation.

The TS section of the TSE2004av device uses a pointer register to access all registers in the device. Additionally, all data transfers to and from this section of the device are performed as block read/write operations. The data is transmitted/received as 2 bytes, Most Significant Byte (MSB) first, and terminated with a NoAck and STOP after the Least Significant byte (LSB). Data and address information is transmitted and received Most Significant Bit first.

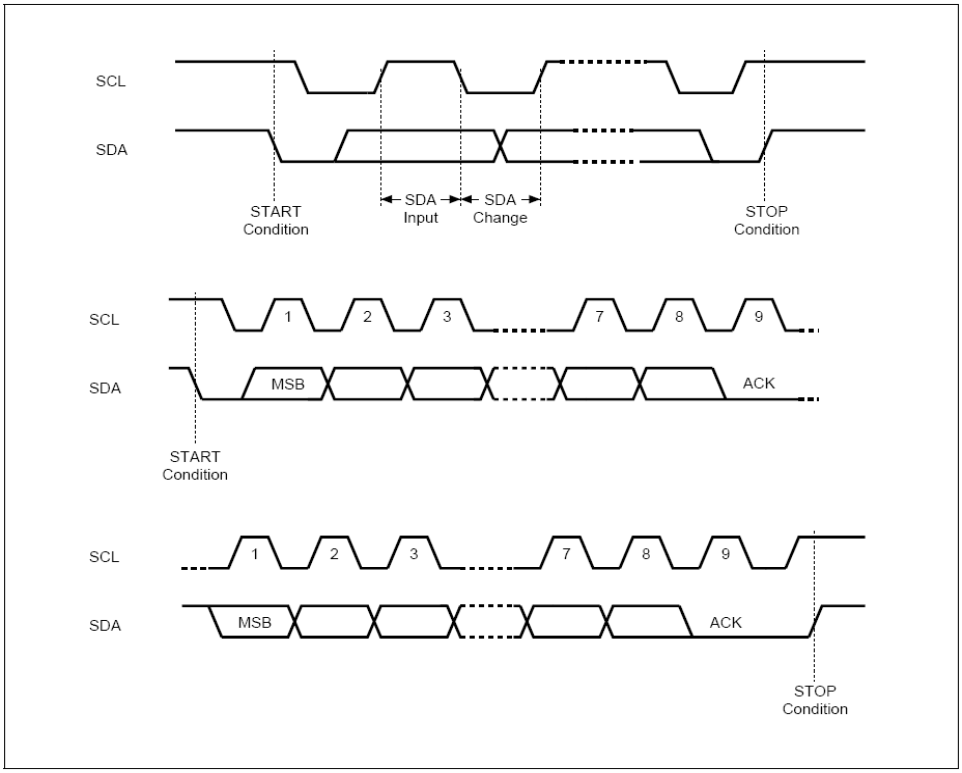


Figure 2 — I^{2}C Bus Protocol

Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the EE into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle for the EE. Neither of these conditions changes the operation of the TS section of a TSE2004av.

Acknowledge Bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits.

No Acknowledge Bit (NACK)

The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

Data Input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change only when Serial Clock (SCL) is driven Low.

Memory Addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 2 (on Serial Data (SDA), most significant bit first).

Table 2 — Device Select Code

Function	Abbr	Device Type Identifier[1]				Select Address[2, 4]			R/W_n	SA0 Pin[3]
		b7	b6	b5	b4	b3	b2	b1	b0	
Read Temperature registers[8]	RTR	0	0	1	1	LSA2	LSA1	LSA0	1	0 or 1
Write Temperature registers[8]	WTR								0	
Read EE memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE memory	WSPD								0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0	RPS0					0	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 1	RPS1					1	0	0	1	0, 1 or V_{HV}
Read Protection Status, block 2	RPS2					1	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 3	RPS3					0	0	0	1	0, 1 or V_{HV}
Set EE Page Address to 0[5, 10]	SPA0					1	1	0	0	0, 1 or V_{HV}
Set EE Page Address to 1[5, 10]	SPA1					1	1	1	0	0, 1 or V_{HV}
Read EE Page Address[6]	RPA					1	1	0	1	0, 1 or V_{HV}
Reserved	--					All Other Encodings				

Note 1: The most significant bit, b7, is sent first.
Note 2: Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins; see Figure 2 on page 6.
Note 3: SA0 pin is driven to 0 = V_{SSSPD}, 1 = V_{DDSPD}, or V_{HV}.
Note 4: For backward compatibility with previous devices, the order of block select bits (b3 and b1) are not a simple binary encoding of the block number.
Note 5: Set EE page address to 0 selects the lower 256 bytes of EEPROM, setting to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.
Note 6: Reading the EE page address results in Ack when the current page is 0 and NoAck when the current page is 1.
Note 7: Permanent Write Protect features of the EE1002(A) and TSE2002av have been eliminated from the EE/TSE devices.
Note 8: TSE2004av only.
Note 9: Don't Care values for word address and data fields following commands may result in Ack or No_Ack responses from EE/TSE devices. See Figure 6, "Protocol for Commands SWPn, CWP, RPSn, SPAn, RPA," on page 12.
Note 10. No delay is required after switching pages via the SPAn commands before accessing the device.

The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address. To address the EE memory array, the 4-bit Device Type Identifier is 1010b; to access the write-protection settings or EE page address, it is 0110b; and to access the Temperature Sensor settings is 0011b (TSE2004av only). Additionally, writing or clearing the reversible EE write protect requires that SA0 be raised to the V_{HV} voltage level.

Up to eight EE/TSE devices can be connected on a single I^2C Bus. Each one is given a unique 3-bit Logical Serial Address code. The LSA is a decoding of information on the SA pins SA0, SA1, and SA2 as described in Table 2 on page 6. When the Device Select Code is received, the device only responds if the Select Address is the same as the Logical Serial Address.

Write Protection commands SWPn, CWP, and RPSn, and the EE Page Address commands SPAn and RPA, do not use the Select Address or Logical Serial Address, therefore all devices on the I^2C Bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used for external device programmers rather than in-system applications.

The 8th bit is the Read/Write bit (R/W_n). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the EE Device Select code, the EE section deselects itself from the bus, and goes into Standby mode. The I^2C Bus operating modes are detailed in Table 3.

Table 3 — I^2C Bus Operating Modes

Mode	R/W_n Bit	Bytes	Initial Sequence
EE Current Address Read	1	1	START, Device Select, R/W_n = 1
EE Random Address Read	0	1	START, Device Select, R/W_n = 0, Address
	1		reSTART, Device Select, R/W_n = 1
EE Sequential Read	1	≥ 1	Similar to Current or Random Address Read
EE Byte Write	0	1	START, Device Select, R/W_n = 0, data, STOP
EE Page Write	0	≤ 16	START, Device Select, R/W_n = 0, data, STOP
TS Write[1]	0	2	START, Device Select, R/W_n=0, pointer, data, STOP
TS Read[1]	1	2	START, Device Select, R/W_n=1, pointer, data, STOP

Note:
1. TSE2004av only

2.5.Device Pin Definition

Table 4 — Pin Description for EE/TSE

Pin #	Pin Name	Type	Definition
1	SA0	Input	Select Address 0
2	SA1	Input	Select Address 1
3	SA2	Input	Select Address 2
4	V_{SSSPD}	Supply	Ground
5	SDA	Input/Open Drain Output	Serial data
6	SCL	Input	Serial clock
7	EVENT_n	Open Drain Output	TSE2004av temperature event
	No Connect	No Connect	EE1004-v does not use this pin
8	V_{DDSPD}	Supply	Supply voltage
Note: Thermal sensing devices also have a heat paddle, typically connected to the application ground plane			

2.6.Pin Functional Description

Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DDSPD}. (Figure 3 on page 9 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{DDSPD} in the I^2C Bus chain. (Figure 3 on page 9 indicates how the value of the pull-up resistor can be calculated).

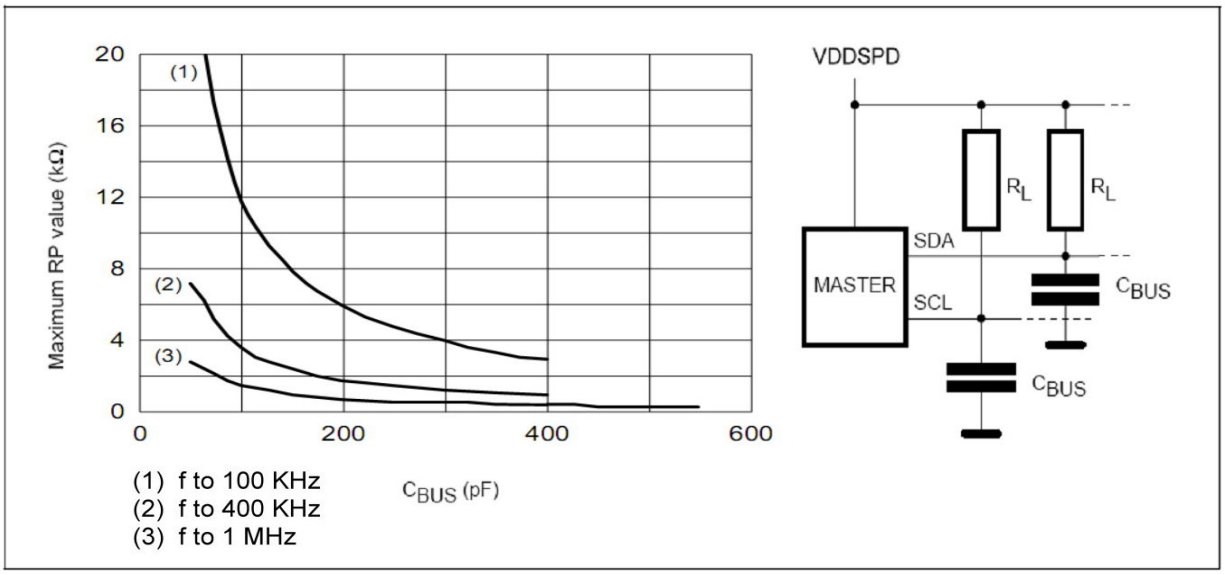


Figure 3 — Maximum R_L Value Versus Bus Capacitance (C_{BUS}) for an I^2C Bus

Serial Address SA (SA0, SA1, SA2)

These input signals are used to create the Logical Serial Address LSA that is compared to the three least significant bits (b3, b2, b1) of the 7-bit Slave Address. See Table 1 on page 4 for details on LSA encoding.

The SA0 input is also used to detect the V_{HV} voltage when decoding an SWPn or CWP instruction. Refer to Table 3 on page 7 for decode details.

EVENT_n (TSE2004av only)

The TSE2004av EVENT_n pin is an open drain output that requires a pull-up to V_{DDSPD} on the system motherboard or integrated into the master controller. EVENT_n has three operating modes, depending on configuration settings and any current out-of-limit conditions. These modes are Interrupt, Comparator, or TCRIT Only.

In Interrupt Mode the EVENT_n pin will remain asserted until it is released by writing a ‘1’ to the “Clear Event” bit in the Status Register. The value to write is independent of the EVENT_n polarity bit.

In Comparator Mode the EVENT_n pin will clear itself when the error condition that caused the pin to be asserted is removed. When the temperature is compared against the TCRIT limit, then this mode is always used.

Finally, in the TCRIT Only Mode the EVENT_n pin will only be asserted if the measured temperature exceeds the TCRIT Limit. Once the pin has been asserted, it will remain asserted until the temperature drops below the TCRIT Limit minus the TCRIT hysteresis. Figure 5 illustrates the operation of the different modes over time and temperature.

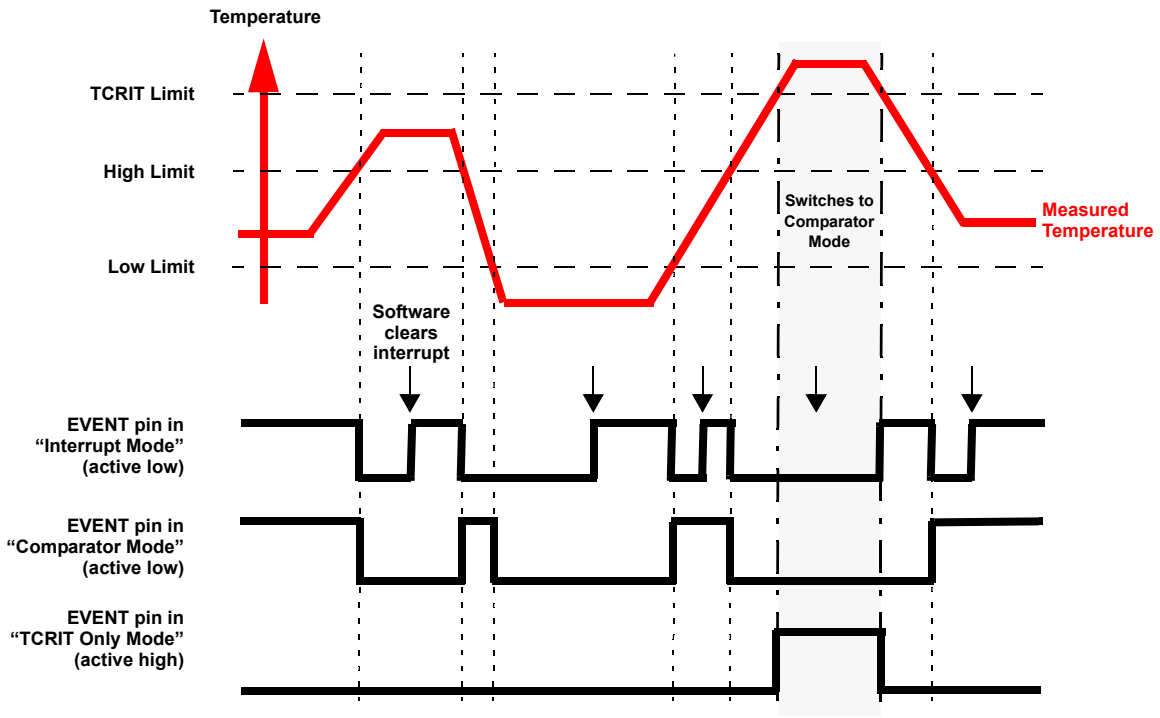


Figure 4 — EVENT_n Pin Mode functionality

Systems that use the active high mode for EVENT_n must be wired point to point between the TSE2004av and the sensing controller. Wire-OR configurations should not be used with active high EVENT_n since any device pulling the EVENT_n signal low will mask the other devices on the bus. Also note that the normal state of EVENT_n in active high mode is a 0 which will constantly draw power through the pull-up resistor.

2.7. EE/TSE Device Reset and Initialization

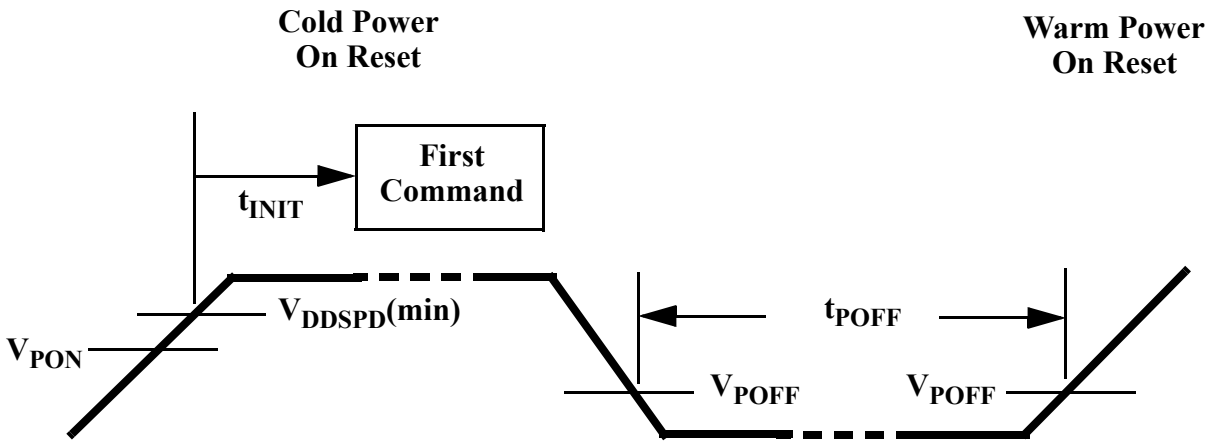


Figure 5 — V_{DDSPD} Ramp Up and Ramp Down

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, V_{DDSPD} must rise monotonically between V_{PON} and V_{DDSPD}(min) without ringback to ensure proper startup. Once V_{DDSPD} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{DDSPD} voltage must be applied, and no command may be issued to the device for t_{INIT}. The supply voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

At power down (phase during which V_{DDSPD} decreases continuously), as soon as V_{DDSPD} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. On warm power cycling, V_{DDSPD} must remain below V_{POFF} for t_{POFF}, and must meet cold power on reset timing when restoring power.

The EE/TSE devices are delivered with all bits in the EEPROM memory array set to '1' (each byte contains 0xFF).

2.8. EE/TSE Software Write Protect

The EE/TSE devices have three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0

- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 1

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

SWPn and CWP: Set and Clear Write Protection

If the software write-protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears write protection for all blocks.

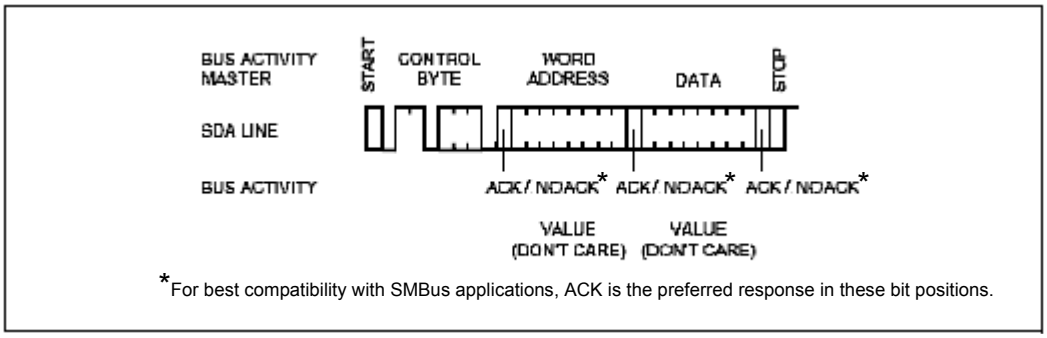


Figure 6 — Protocol for Commands SWPn, CWP, RPSn, SPAn, RPA

RPSn: Read Protection Status

The controller issues a RPSn command specifying which block to report upon. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck.

SPAn: Set SPD Page Address

The controller issues an SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1). After a cold or warm power-on reset, the SPD Page Address is always 0, selecting the lower 256 bytes.

RPA: Read SPD Page Address

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns Ack) or 1 (device returns NoAck).

2.9. Write Operations

Following a Start condition, the bus master sends a Device Select Code with the R/W_n bit reset to 0. The device acknowledges this, as shown in Table 7 on page 13, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored by the EE, and the EE device does not respond to any requests. For TSE devices, access to the TS portion of the device are permitted during this period.

The device has an internal address counter which is incremented each time a byte is written. If a Write operation is performed to a protected block, the internal address counter is not incremented.

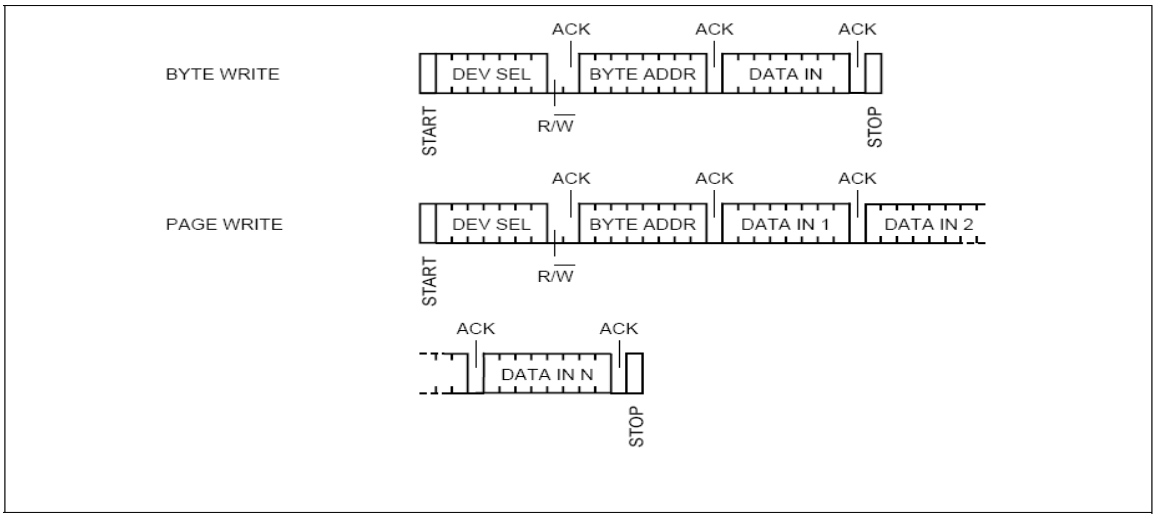


Figure 7 — Write Mode Sequences in a Non-Write Protected Area

Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. After the byte is transferred, the internal byte address counter is incremented unless the block is write protected. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 7 on page 13.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over' occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified.

After each byte is transferred, the internal byte address counter is incremented unless the block is write protected. The transfer is terminated by the bus master generating a Stop condition.

2.10. Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_W) is shown in Table 24 on page 28, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 9, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

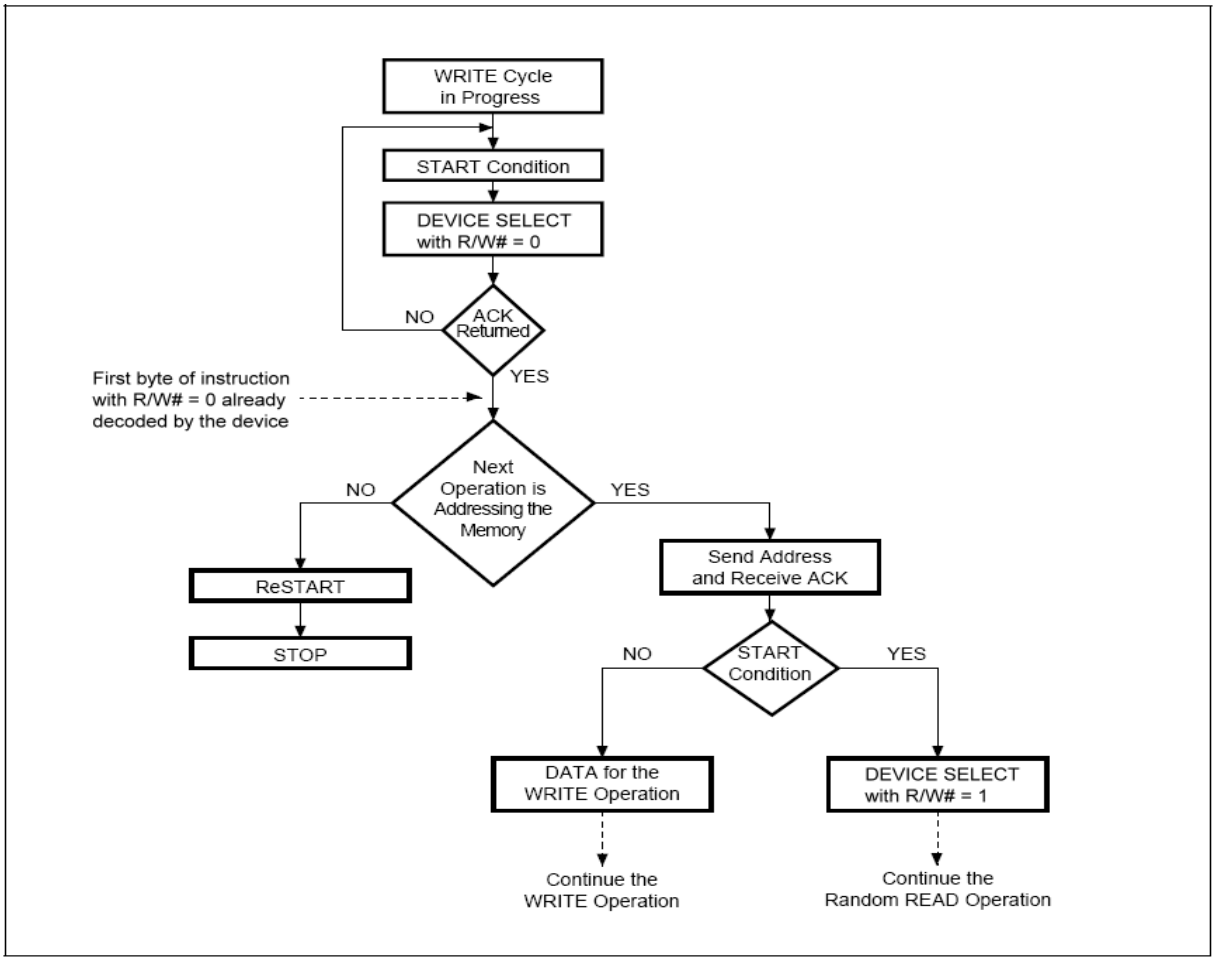


Figure 8 — Write Cycle Polling Flowchart for EE Using ACK

2.11. Read Operations

Read operations are performed independent of the software protection state.

The device has an internal address counter which is incremented each time a byte is read.

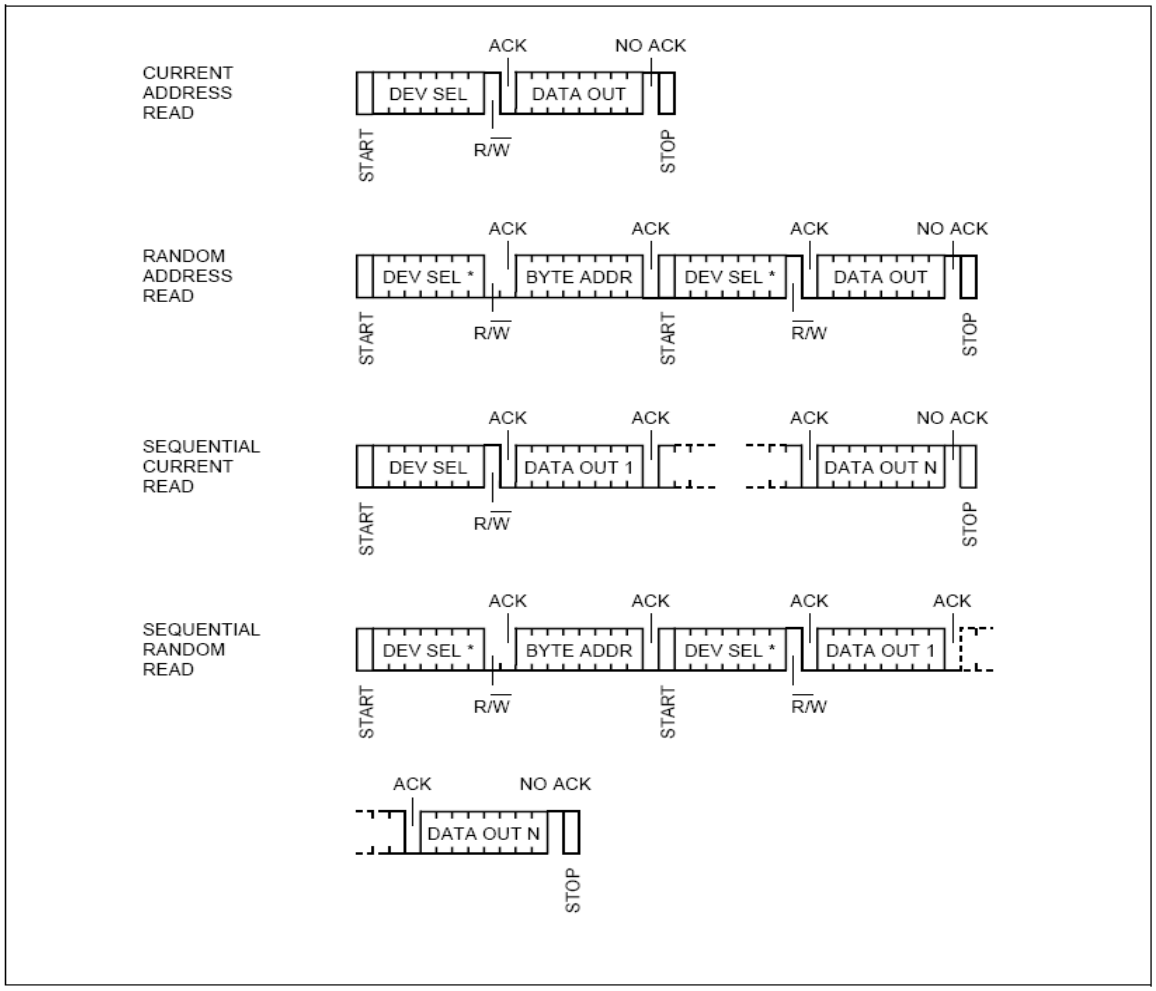


Figure 9 — Read Mode Sequences

Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 10) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R/W_n bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/W_n bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 9 on page 15, without acknowledging the byte.

Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 10.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

Acknowledge in Read Mode

For all Read commands to the SPD, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition. This has no effect on the TS operational status.

Table 5 — Acknowledge When Writing Data or Defining Write Protection (Instructions with R/W_n bit = 0)

Status	Instruction	Ack	Address	Ack	Data byte	Ack	Write Cycle (t_W)
Protected with SWPn	SWPn	NoAck	Not significant	NoAck	Not significant	NoAck	No
	CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write in protected block	Ack	Address	Ack	Data	NoAck	No
Not protected	SWPn or CWP	Ack	Not significant	Ack	Not significant	Ack	Yes
	Page or byte write	Ack	Address	Ack	Data	Ack	Yes

Table 6 — Acknowledge When Reading the Protection Status (Instructions with R/W_n bit = 1)

SWPn Status	Instruction	ACK	Address	ACK	Data byte	ACK
Set	RPSn	NoAck	Not significant	NoAck	Not significant	NoAck
Not Set	RPSn	Ack	Not significant	NoAck	Not significant	NoAck
Note: X = Set or Not Set.						

2.12. Temperature Sensor (TS) Device Operation (TSE2004av only)

The TSE2004av Temperature Register Set is accessed though the I^2C Bus address 0011_bbb_R/W_n. The “bbb” denotes the Logical Serial Address code LSA. In the event SA0 is in the high voltage state, the device shall not recognize the LSA.

The Temperature Register Set stores the temperature data, limits, and configuration values. All registers in the address space from 0x00 through 0x08 are 16-bit registers (see section 2.15 for detailed information), accessed through block read and write commands.

Behavior on accesses to invalid register locations is vendor-specific and may return an Ack or a NoAck.

2.13. TS Write Operations

Writing to the TSE2004av Temperature Register Set is accomplished through a modified block write operation for two (2) data bytes. To maintain I^2C Bus compatibility, the 16 bit register is accessed through a pointer register, requiring the write sequence to include an address pointer in addition to the Slave address. This indicates the storage location for the next two bytes received. Figure 11 shows an entire write transaction on the bus.

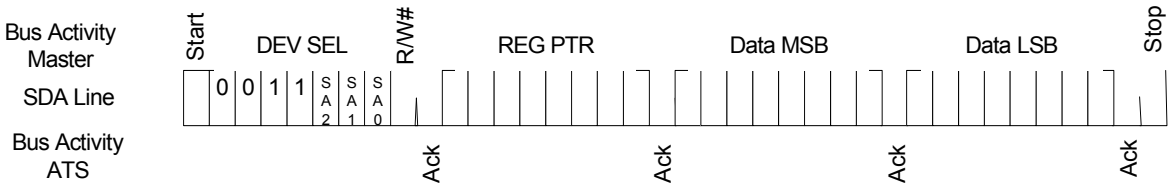


Figure 10 — TS Register Write Operation

2.14. TS Read Operations

Reading data from the TS may be accomplished in one of two ways:

1. If the location latched in the Pointer Register is correct (for normal operation it is expected the same address will be read repeatedly for temperature), the read sequence may consist of a Slave Address from the bus master followed by two bytes of data from the device; or

2. The pointer register is loaded with the correct register address, and the data is read. The sequence to preset the pointer register is shown in Figure 12, and the preset pointer read is shown in Figure 13. If it is desired to read random address each cycle, the complete Pointer Write, Word Read sequence is shown in Figure 14.

The data byte has the most significant bit first. At the end of a read, this device can accept either Acknowledge (Ack) or No Acknowledge (No Ack) from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

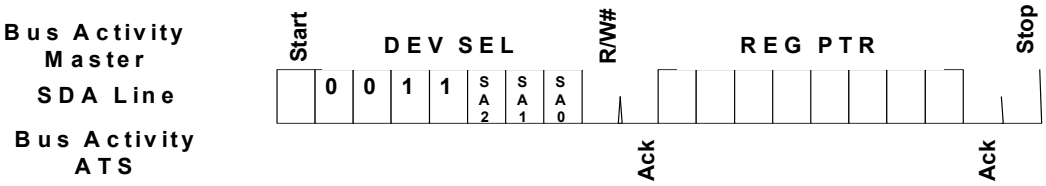


Figure 11 — I^2C Bus Write to Pointer Register

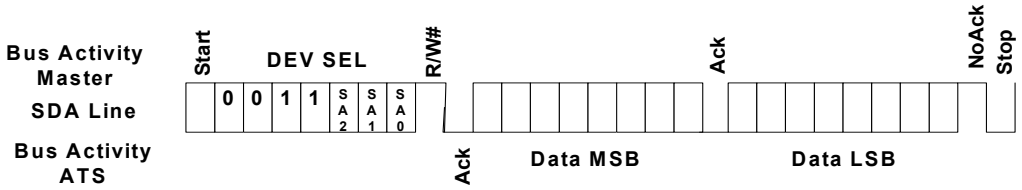


Figure 12 — I²C Bus Preset Pointer Register Word Read

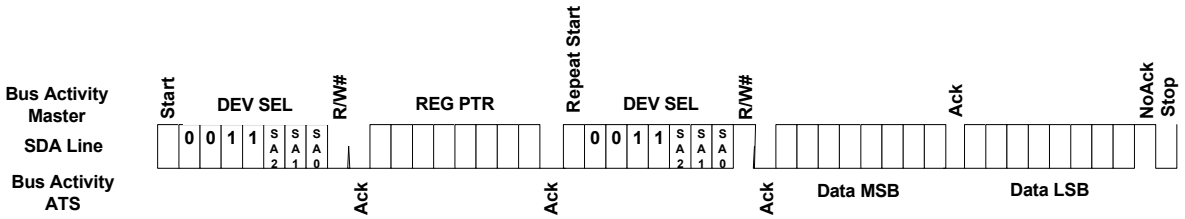


Figure 13 — I²C Bus Pointer Write Register Word Read

2.15. TS Register Set Definition

The register set address are shown in Table 4. These values are used in the I²C Bus operations as the "REG_PTR" in Figures 10 through 13.

Table 7 — Temperature Register Addresses

ADDR	R/W	NAME	FUNCTION	DEFAULT
N/A	W	Address Pointer	Address storage for subsequent operations	undefined
00	R	Capabilities	Indicates the functions and capabilities of the temperature sensor	N/A
01	R/W	Configuration	Controls the operation of the temperature monitor	0000
02	R/W	High Limit	Temperature High Limit	0000
03	R/W	Low Limit	Temperature Low Limit	0000
04	R/W	TCRIT Limit	Critical Temperature	0000
05	R	Ambient Temperature	Current Ambient temperature	N/A
06	R	Manufacturer ID	PCI-SIG manufacturer ID	undefined
07	R	Device/Revision	Device ID and Revision number	22xx
08-0F	R/W	Vendor-defined	Vendor specific information	N/A

2.16. TS Capabilities Register

Table 8 — TS Capabilities Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0
00	R	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
		EVSD	TMOUT	VHV	TRES[1:0]		RANGE	ACC	EVENT

The TS Capabilities Register indicates the supported features of the temperature sensor portion of the TSE2004av. This register is read-only and writing to it will have no effect.

Bits 15 - Bit 8 - RFU - Reserved for future use. These bits will always read ‘0’

Bit 7 - EVSD - EVENT_n with Shutdown action. Must be 1.

‘0’ - Not used.

‘1’ - The EVENT_n output is deasserted (not driven) when entering shutdown, and remains deasserted upon exit from shutdown until the next thermal sample is taken, or possibly sooner if EVENT_n is programmed for comparator mode. In interrupt mode, EVENT_n may or may not be asserted when exiting shutdown if a pending interrupt has not been cleared.

Bit 6 - TMOUT - Bus timeout period during normal operation. Must be 1.

‘0’ - Not used.

‘1’ - Parameter $t_{TIMEOUT}$ is supported within the range of 25 to 35 ms.

Bit 5 - VHV

‘0’ - Not used.

‘1’ - Defined for compatibility with TS3000 devices; since all EE/TSE devices are required to support V_{HV}, this bit is not used.

Bits 4 - 3 - TRES[1:0] - Indicates the resolution of the temperature monitor as shown in Table 9 on page 19

Table 9 — TRES Bit Decode

TRES[1:0]		TEMPERATURE RESOLUTION
1	0	
0	0	0.5 °C (9-bit)
0	1	0.25 °C (10-bit)
1	0	0.125 °C (11-bit)
1	1	0.0625 °C (12-bit)

Bit 2 - RANGE - Indicates the supported temperature range.

‘0’ - Not used.

‘1’ - The temperature monitor can read temperatures below 0 °C and sets the sign bit appropriately.

Bit 1 - ACC - Indicates the supported temperature accuracy.

‘0’ - Not used.

'1' - The temperature monitor has ±1 °C accuracy over the active range (75 °C to 95 °C) and 2°C accuracy over the monitoring range (40 °C to 125 °C)

Bit 0 - EVENT - Indicates whether the temperature monitor supports interrupt capabilities

'0' - Not used.

'1' - The device supports interrupt capabilities.

2.17. TS Configuration Register

Table 10 — TS Configuration Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
01	R/W	RFU	RFU	RFU	RFU	RFU	HYST[1:0]		SHDN	0000
		TCRIT_ LOCK	EVENT _LOCK	CLEAR	EVENT _ STS	EVENT _CTRL	TCRIT_ ONLY	EVENT _ POL	EVENT _MODE	

The TS Configuration Register holds the control and status bits of the EVENT_n pin as well as general hysteresis on all limits. To avoid glitches on the EVENT_n output pin, users should disable EVENT or TCRIT functions prior to programming or changing other device configuration settings.

Bits 15 - 11 - RFU - Reserved for future use. These bits will always read '0' and writing to them will have no affect. For future compatibility, all RFU bits must be programmed as '0'.

Bits 10 - 9 - HYST[1:0] - Control the hysteresis that is applied to all limits as shown in Table 11 on page 20. This hysteresis applies to all limits when the temperature is dropping below the threshold so that once the temperature is above a given threshold, it must drop below the threshold minus the hysteresis in order to be flagged as an interrupt event. Note that hysteresis is also applied to EVENT_n pin functionality. When either of the lock bits is set, these bits cannot be altered.

Table 11 — HYST Bit Decode

HYST[1:0]		HYSTERESIS
1	**0**	
0	0	disable hysteresis (default)
0	1	1.5 °C
1	0	3 °C
1	1	6 °C

Bit 8 - SHDN - Shutdown. The thermal sensing device and A/D converter are disabled to save power, no events will be generated. When either of the lock bits is set, this bit cannot be set until unlocked. However it can be cleared at any time. When in shutdown mode, TSE2004 devices still respond to commands normally, however bus timeout may or may not be supported in this mode.

'0' (default) - The thermal sensor is active and converting.

'1' - The thermal sensor is disabled and will not generate interrupts or update the temperature data.

Bit 7 - TCRIT_LOCK - Locks the TCRIT Limit Register from being updated.

'0' (default) - The TCRIT Limit Register can be updated normally.

'1' - The TCRIT Limit Register is locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 6 - EVENT_LOCK - Locks the High and Low Limit Registers from being updated.

'0' (default) - The High and Low Limit Registers can be updated normally.

'1' - The High and Low Limit Registers are locked and cannot be updated. Once this bit has been set, it cannot be cleared until an internal power on reset.

Bit 5 - CLEAR - Clears the EVENT_n pin when it has been asserted. This bit is write only and will always read '0'.

'0' - does nothing

'1' - The EVENT_n pin is released and will not be asserted until a new interrupt condition occurs. This bit is ignored if the device is operating in Comparator Mode. This bit is self clearing.

Bit 4 - EVENT_STS - Indicates if the EVENT_n pin is asserted. This bit is read only.

'0' (default) - The EVENT_n pin is not being asserted by the device.

'1' - The EVENT_n pin is being asserted by the device.

Bit 3 - EVENT_CTRL - Masks the EVENT_n pin from generating an interrupt. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default) - The EVENT_n pin is disabled and will not generate interrupts.

'1' - The EVENT_n pin is enabled.

Bit 2 - TCRIT_ONLY - Controls whether the EVENT_n pin will be asserted from a high / low out-of-limit condition. When the EVENT_LOCK bit is set, this bit cannot be altered.

'0' (default) - The EVENT_n pin will be asserted if the measured temperature is above the High Limit or below the Low Limit in addition to if the temperature is above the TCRIT Limit.

'1' - The EVENT_n pin will only be asserted if the measured temperature is above the TCRIT Limit.

Bit 1 - EVENT_POL - Controls the "active" state of the EVENT_n pin. The EVENT_n pin is driven to this state when it is asserted. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default) - The EVENT_n pin is active low. The "active" state of the pin will be logical '0'.

'1' - The EVENT_n pin is active high. The "active" state of the pin will be logical '1'.

Bit 0 - EVENT_MODE - Controls the behavior of the EVENT_n pin. The EVENT_n pin may function in either comparator or interrupt mode. If either of the lock bits are set (bit 7 and bit 6), then this bit cannot be altered.

'0' (default) - The EVENT_n pin will function in comparator mode

'1' - The EVENT_n pin will function in interrupt mode

2.18. TSE2004av Temperature Register Value Definitions

Temperatures in the High Limit Register, Low Limit Register, TCRIT Register, and Temperature Data Register are expressed in two's complement format. Bits B12 through B2 for each of these registers are defined for all device resolutions as defined in the TRES field of the Capabilities Register, hence a 0.25 °C minimum granularity is supported in

all registers. Examples of valid settings and interpretation of temperature register bits are shown in Table .

Table 12 — Temperature Register Coding Examples

B15~B0 (binary)	Value	Units
xxx0 0000 0010 11xx	+2.75	°C
xxx0 0000 0001 00xx	+1.00	°C
xxx0 0000 0000 01xx	+0.25	°C
xxx0 0000 0000 00xx	0	°C
xxx1 1111 1111 11xx	-0.25	°C
xxx1 1111 1111 00xx	-1.00	°C
xxx1 1111 1101 01xx	-2.75	°C

The TRES field of the Capabilities Register optionally defines higher resolution devices. For compatibility and simplicity, this additional resolution affects only the Temperature Data Register but none of the Limit Registers. When higher resolution devices generate status or EVENT_n changes, only bits B12 through B2 are used in the comparison; however, all 11 bits (TRES[1-0] = 10) or all 12 bits (TRES[1-0] = 11) are visible in reads from the Temperature Data Register.

When a lower resolution device is indicated in the Capabilities Register (TRES[1-0] = 00), the finest resolution supported is 0.5 °C. When this is detected, bit 2 of all Limit Registers should be programmed to 0 to assure correct operation of the temperature comparators.

2.19. High Limit Register

The temperature limit registers (High, Low, and TCrit) define the temperatures to be used by various on-chip comparators to determine device temperature status and thermal EVENTs. For future compatibility, unused bits "-" must be programmed as 0.

Table 13 — High Limit Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
02	R/W	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

The High Limit Register holds the High Limit for the nominal operating window. When the temperature rises above the High Limit, or drops below or equal to the High Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 10 on page 20), then this register becomes read-only.

2.20. Low Limit Register

Table 14 — Low Limit Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
03	R/W	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

The Low Limit Register holds the lower limit for the nominal operating window. When the temperature drops below the Low Limit or rises up to meet or exceed the Low Limit, then the EVENT_n pin is asserted (if enabled). If the EVENT_LOCK bit is set in the Configuration Register see Table 10 on page 20), then this register becomes read-only.

2.21. TCRIT Limit Register

T

Table 15 — TCRIT Limit Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
04	R/W	-	-	-	Sign	128	64	32	16	
		8	4	2	1	0.5	0.25	-	-	

The TCRIT Limit Register holds the TCRIT Limit. If the temperature exceeds the limit, the EVENT_n pin will be asserted. It will remain asserted until the temperature drops below or equal to the limit minus hysteresis. If the TCRIT_LOCK bit is set in the Configuration Register (see Table 10 on page 20), then this register becomes read-only.

2.22. Temperature Data Register

Table 16 — Temperature Data Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
05	R	TCRIT	HIGH	LOW	Sign	128	64	32	16	N/A (0000)
		8	4	2	1	0.5	0.25*	0.125*	0.0625*	
*: Resolution defined based on value of TRES field of the Capabilities Register. Unused/unsupported bits will read as 0.										

The Temperature Data Register holds the 10-bit + sign data for the internal temperature measurement as well as the status bits indicating which error conditions, if any, are active. The encoding of bits B12 through B0 is the same as for the temperature limit registers.

Bit 15 - TCRIT - When set, the temperature is above the TCRIT Limit. This bit will remain set so long as the temperature is above TCRIT and will automatically clear once the temperature has dropped below the limit minus the hysteresis.

Bit 14 - HIGH - When set, the temperature is above the High Limit. This bit will remain set so long as the temperature is above the HIGH limit. Once set, it will only be cleared when the temperature drops below or equal to the HIGH Limit minus the hysteresis.

Bit 13 - LOW - When set, the temperature is below the Low Limit. This bit will remain set so long as the temperature is below the Low Limit minus the hysteresis. Once set, it will only be cleared when the temperature meets or exceeds the Low Limit.

2.23.TSE2004av Manufacturer ID Register

Table 17 — TSE Manufacturer ID Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
06	R/W	X	X	X	X	X	X	X	X	XXXX
		X	X	X	X	X	X	X	X	

The Manufacturer ID Register holds the PCI SIG number assigned to the specific manufacturer. This register is not available on EE1004-v devices.

2.24. TSE2004av Device ID / Revision Register

Table 18 — TSE Device ID / Revision Register

ADDR	R/W	B15 / B7	B14 / B6	B13 / B5	B12 / B4	B11 / B3	B10 / B2	B9 / B1	B8 / B0	DEFAULT
07	R/W	0	0	1	0	0	0	1	0	22XX
		X	X	X	X	X	X	X	X	

The upper byte of the Device ID / Revision Register must be 0x22 for the TSE2004av. The lower byte holds the revision value which is vendor-specific. This register is not available on EE1004-v devices.

3. PARAMETRIC CHARACTERISTICS

3.1. Maximum Ratings

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 19 — Absolute Maximum Ratings for EE1004-v and TSE2004av

Symbol	Parameter	Min	Max	Units
T_{STG}	Storage temperature	-65	150	°C
V_{IO}	Input or output range, SA0	-0.50	10.0	V
	Input or output range, other pins	-0.50	4.3	V
V_{DDSPD}	Supply voltage	-0.5	4.3	V

3.2. DC and AC Parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the EE/TSE devices. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 20 — Operating Conditions for EE1004-v and TSE2004av

Symbol	Parameter	EE1004-1, TSE2004a1		EE1004-2, TSE2004a2		Units
		Min	Max	Min	Max	
V_{DDSPD}	Supply Voltage	1.7	3.6	2.2	3.6	V
T_C	Case operating temperature	0	95	0	95	°C

Table 21 — AC Measurement Conditions for EE1004-v and TSE2004av

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2 * V_{DDSPD} to 0.8 * V_{DDSPD}		V
	Input and output timing reference levels	0.3 * V_{DDSPD} to 0.7 * V_{DDSPD}		V

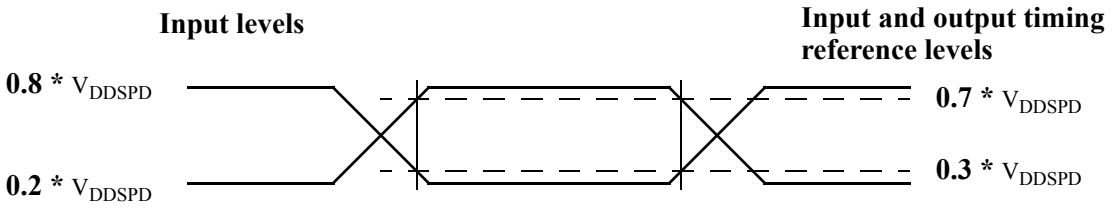


Figure 14 — AC Measurement I/O Waveform

Table 22 — Input Parameters for EE1004-v and TSE2004av

Symbol	Parameter[1,2]	Test Condition	Min	Max	Units
C_{IN}	Input capacitance (SDA)	--	--	8	pF
C_{IN}	Input capacitance (other pins)	--	--	6	pF
Z_{EIL}	Ei (SA0, SA1, SA2) input impedance	$V_{IN} < 0.3 * V_{DDSPD}$	30	--	kΩ
Z_{EIH}	Ei (SA0, SA1, SA2) input impedance	$V_{IN} > 0.7 * V_{DDSPD}$	800	--	kΩ
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	Single glitch, f ≤ 100 KHz	--	--	ns
		Single glitch, f > 100 KHz	0	50	

Note 1: T_A = 25 °C, f = 400 kHz
Note 2: Verified by design and characterization, not necessarily tested on all devices

DC Characteristics are listed separately for the wide voltage range EE/TSE devices.

Table 23 — DC Characteristics for EE1004-v and TSE2004av

Sym	Parameter	Test Condition (in addition to those in Table 20 on page 25)	f ≤ 400KHz		f > 400 KHz		Units
			Min	Max	Min	Max	
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}	--	±5	--	±5	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SSSPD}$ or V_{DDSPD}, SDA in Hi-Z	--	±5	--	±5	µA
I_{DDR}	Supply current, read operation	V_{DDSPD} = 3.3 V, f_C = 1 MHz	--	2	--	2	mA
I_{DDW}	Supply current, write operation	V_{DDSPD} = 3.3 V, f_C = 1 MHz	--	3	--	3	mA
I_{DD1}	Standby Supply current	$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, V_{DDSPD} = 3.6 V	--	100	--	100	µA
		$V_{IN} = V_{SSSPD}$ or V_{DDSPD}, V_{DDSPD} = 1.7 V	--	100	--	100	µA
V_{IL}	Input low voltage (SCL, SDA)	--	-0.5	0.3 * V_{DDSPD}	-0.5	0.3 * V_{DDSPD}	V
V_{IH}	Input high voltage (SCL, SDA)	--	0.7 * V_{DDSPD}	V_{DDSPD} + 0.5	0.7 * V_{DDSPD}	V_{DDSPD} + 0.5	V
V_{HV}	SA0 high voltage	$V_{HV} - V_{DDSPD} \geq 4.8$ V	7	10	7	10	V
V_{OL1}	Output low voltage[1] open-drain or open-collector	3 mA sink current, $V_{DDSPD} > 2$ V	--	0.4	--	0.4	V
V_{OL2}		2 mA sink current, $V_{DDSPD} \leq 2$ V	--	0.2 * V_{DDPSD}	--	0.2 * V_{DDPSD}	V
IOL	LOW-level output current[2]	VOL = 0.4 V	3		20		mA
		VOL = 0.6 V	6		--		mA
V_{HYST}	Input hysteresis	$V_{DDSPD} < 2$ V	0.10 * V_{DDSPD}	--	0.10 * V_{DDSPD}	--	V
		$V_{DDSPD} \geq 2$ V	0.05 * V_{DDSPD}	--	0.05 * V_{DDSPD}	--	V
V_{PON}	Power On Reset threshold	Monotonic rise between V_{PON} and V_{DDSPD}(min) without ringback	1.6	--	1.6	--	V
V_{POFF}	Power Off threshold for warm power on cycle	No ringback above V_{POFF}	--	0.9	--	0.9	V

Notes:

1. The same resistor value to drive 3 mA at 3.0 V V_{DDSPD} provides the same RC time constant when using < 2 V V_{DDSPD} with a smaller current draw.

2. In order to drive full bus load at 400 KHz, 6 mA I_{OL} is required at 0.6 V V_{OL}. Parts not meeting this specification can still function, but not at 400 KHz and 400 pF.

Table 24 — AC Characteristics for EE1004-v and TSE2004av

		V_{DDSPD} < 2.2 V[4]		$V_{DDSPD} \geq$ 2.2 V				
		100 KHz[10]		400 KHz[9]		1000 KHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{SCL}	Clock frequency	10	100	10	400	10	1000	kHz
t_{HIGH}	Clock pulse width high time	4000	--	600	--	260	--	ns
t_{LOW}[6]	Clock pulse width low time	4700	--	1300	--	500	--	ns
$t_{TIMEOUT}$[5,7]	Detect clock low timeout	25	35	25	35	25	35	ms
t_R[2]	SDA rise time	--	1000	20	300	--	120	ns
t_F[2]	SDA fall time	--	300	20	300	--	120	ns
$t_{SU:DAT}$	Data in setup time	250	--	100	--	50	--	ns
$t_{HD:DI}$	Data in hold time	0	--	0	--	0	--	ns
$t_{HD:DAT}$	Data out hold time	200	3450	200	900	0	350	ns
$t_{SU:STA}$[1]	Start condition setup time	4700	--	600	--	260	--	ns
$t_{HD:STA}$	Start condition hold time	4000	--	600	--	260	--	ns
$t_{SU:STO}$	Stop condition setup time	4000	--	600	--	260	--	ns
t_{BUF}	Time between Stop Condition and next Start Condition	4700	--	1300	--	500	--	ns
t_W	Write time	--	5	--	5	--	5	ms
t_{POFF}	Warm power cycle off time	1	--	1	--	1	--	ms
t_{INIT}	Time from power on to first command	10	--	10	--	10	--	ms

Note 1: For a reSTART condition, or following a write cycle.
Note 2: Guaranteed by design and characterization, not necessarily tested.
Note 3: To avoid spurious START and STOP conditions, a minimum delay is placed between falling edge of SCL and the falling or rising edge of SDA.
Note 4: V_{DDSPD} below 2.2 V only supported on EE1004-1 and TSE2004a1, not on EE1004-2 or TSE2004a2.
Note 5: Unlike previous EE generations, EE1004-v and TSE2004av families must support bus timeout on EE accesses.
Note 6: EE1004-v and TSE2004av family devices shall not initiate clock stretching, which is an optional I^2C Bus feature.
Note 7: I^2C bus masters can terminate a transaction in process and reset device communication on the bus by asserting SCL low for $t_{TIMEOUT,MAX}$ or longer. EE/TSE devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. EE/TSE devices will not reset if SCL stretching is less than $t_{TIMEOUT,MIN}$. See EE/TSE Bus Timeout Waveforms.
Note 8: EE/TSE devices are not required to support the I^2C Bus ALERT function.
Note 9: 400 KHz timing defined for compatibility with EE1002(A) and TSE2002av applications.
Note 10: 100 KHz timing compliant with SMBus 2.0 specifications.

Table 25 — Temperature-to-Digital Conversion Performance, TSE2004av only

Parameter	Min	Typ	Max	Unit	Test Conditions[3]
Temperature Sensor Accuracy (B grade)[1]	--	±0.5	±1.0	°C	75 °C = T_A = 95 °C, Active Range
	--	±1.0	±2.0	°C	40 °C = T_A = 125 °C, Monitor Range
	--	±2.0	±3.0	°C	-20 °C = T_A = 125 °C
Resolution		0.25		°C	
Conversion Time[2]			125	ms	Worst case conversion time

1 Refer to individual vendor datasheets for explanation of accuracy testing methodology.

2 Assuming 10-bit resolution. Conversion times may range from 62.5 ms for 9-bit to 500 ms for 12-bit accuracy.

3 $V_{DDSPDMIN} \leq V_{DDSPD} \leq V_{DDSPDMAX}$

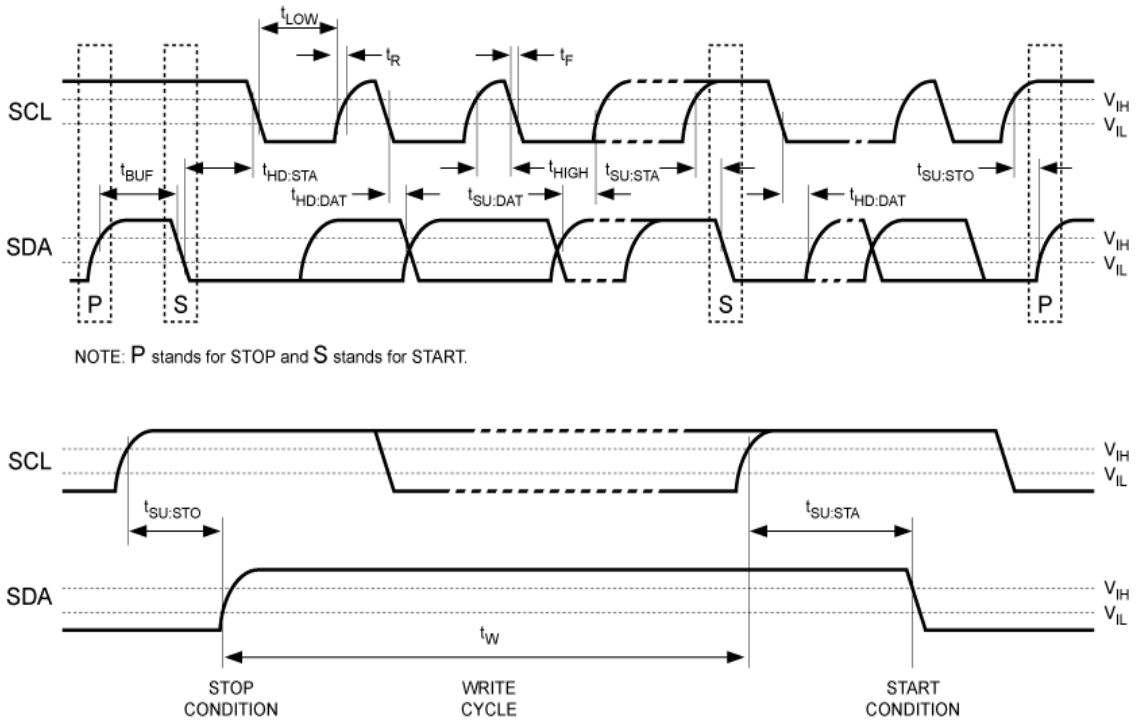


Figure 15 — EE/TSE AC Waveforms

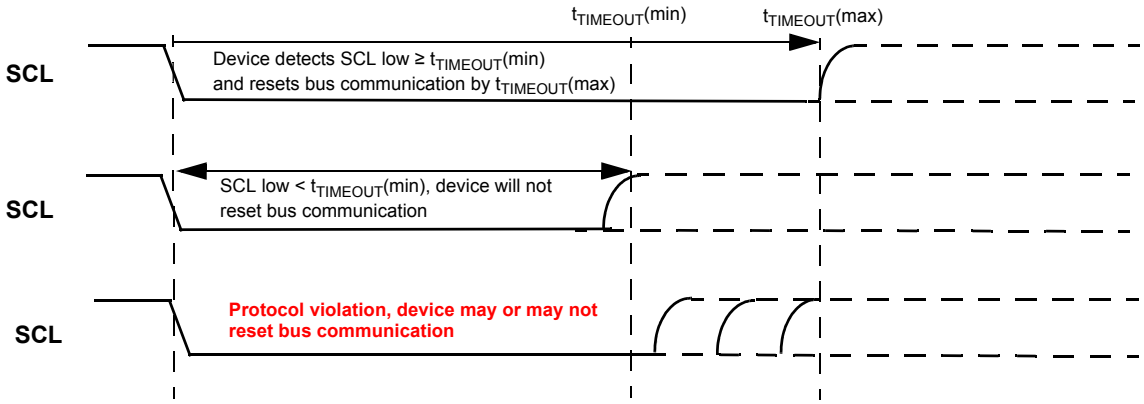


Figure 16 — EE/TSE Bus Timeout Waveforms

4. USE IN A MEMORY MODULE

In the Dual Inline Memory Module (DIMM) application, the EE/TSE is soldered directly onto the printed circuit module. The three Select Address inputs (SA0, SA1, SA2) must be connected to V_{SSSPD} or V_{DDSPD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket. Pull-up resistors needed for normal behavior are connected on the I^2C Bus signals on the motherboard.

Table 26 — DIMM Slot Addressing Modes

DIMM Slot	I^2C Bus Address Compatibility Mode		
	SA2	SA1	SA0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
Note 1: 0 = V_{SSSPD}, 1 = V_{DDSPD}			

TSE2004av only: The EVENT_n pin is expected to be used in a wire-OR configuration with a pull-up resistor to V_{DDSPD} on the motherboard. In this configuration, EVENT_n should be programmed for the active low mode. Also note that comparator mode or TCRIT-only mode for EVENT_n on a wire-OR bus will show the combined results of all devices wired to the EVENT_n signal.

EE/TSE: In DIMM applications, maximum external pull-up resistors on signals are specified based on Figure 3, “Maximum RL Value Versus Bus Capacitance (CBUS) for an I2C Bus,” on page 9. Line capacitance limitations should be calculated using this assumption.

Cap	Res
50 pF	2833 Ω
100 pF	1416 Ω
150 pF	944 Ω
200 pF	708 Ω
250 pF	567 Ω
300 pF	472 Ω
350 pF	405 Ω
400 pF	354 Ω
450 pF	315 Ω
500 pF	283 Ω
550 pF	258 Ω

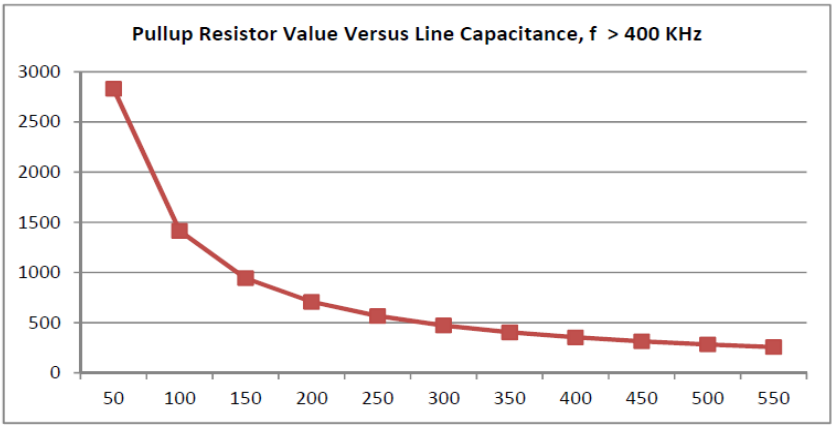


Figure 17 — Pullup Resistor Value Versus line Capacitance

The common landing pattern recommendations for the PSON-8 packaged SPD (EE1002(A)/EE1004-v compatible) or SPD with Thermal Sensor (TSE2002av/TSE2004av compatible) are parameterized to allow for routing design constraints. These apply to the use of devices following MO-229 variations V2030D-3/ W2030D-3/U2030D. The preferred implementation with wide corner pads enhances device centering during assembly, but two narrower options are defined for modules with tight routing requirements. This is included for reference only; please refer to JESD21C-4.1.2 for details.

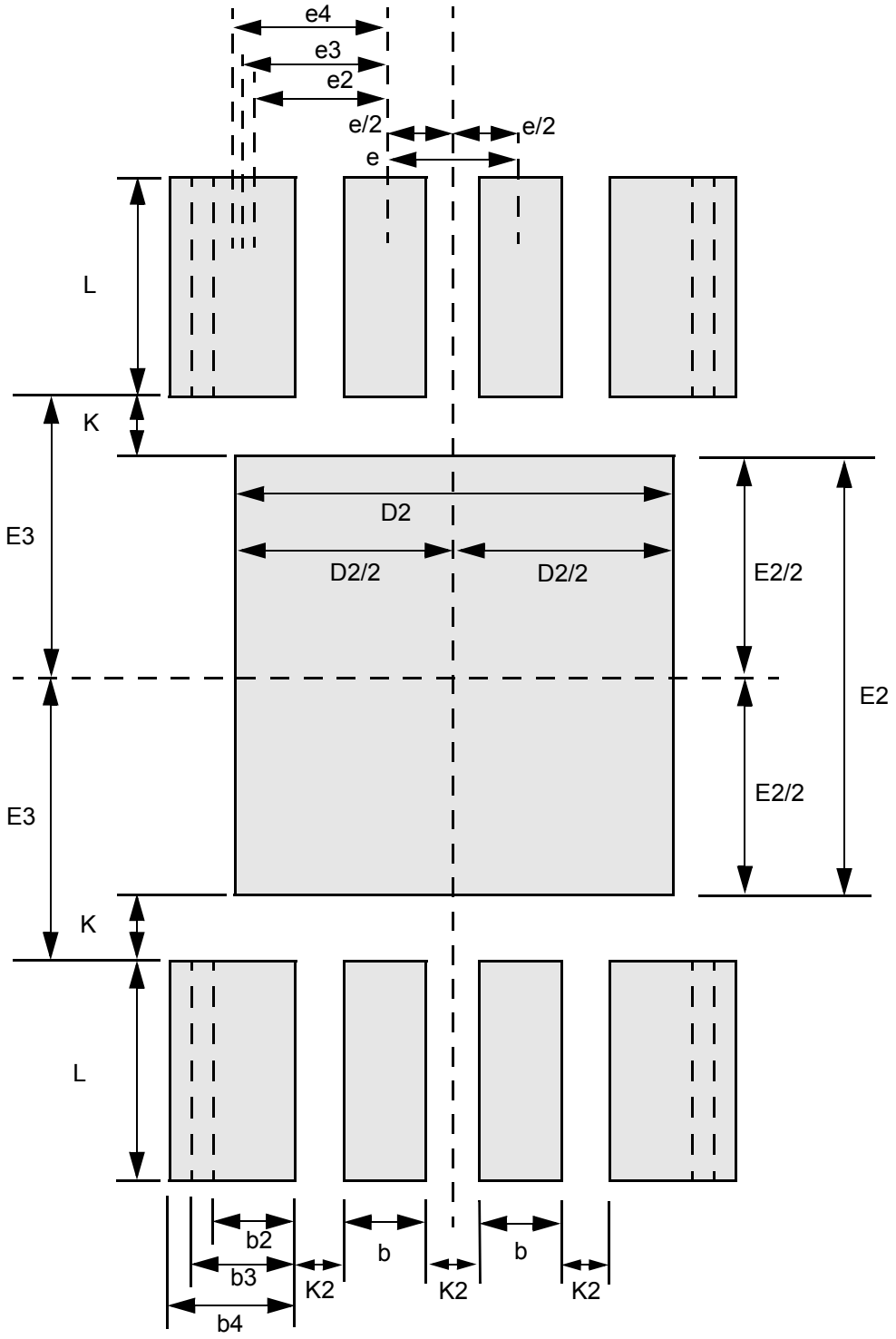


Figure 18 — Common Landing Pattern Recommendations

The table lists three variations of landing pattern implementations, ranked as “Preferred”, “Intermediate”, and “Minimum Acceptable”.

Table 27 — Parameters for SPD Common Landing Pattern

Parameter	Description	Dimension			Notes
		Min	Nom	Max	
D2	Heat paddle width	1.40	-	1.60	
E2	Heat paddle height	1.40	-	1.60	
E3	Heat paddle centerline to contact inner locus	1.00	-	1.05	
L	Contact length	0.70	-	0.80	
K	Heat paddle to contact keepout	0.20	-	-	
K2	Contact to contact keepout	0.20	-	-	
e	Contact centerline to contact centerline pitch for inner contacts	-	0.50	-	
b	Contact width for inner contacts	0.25	-	0.30	
e2	Landing pattern centerline to outer contact centerline, “minimum acceptable” option	-	0.50	-	1
b2	Corner contact width, “minimum acceptable” option	0.25	-	0.30	1
e3	Inner contact centerline to outer contact centerline, “intermediate” option	-	0.55	-	2
b3	Corner contact width, “intermediate” option	0.35	-	0.40	2
e4	Landing pattern centerline to outer contact centerline, “preferred” option	-	0.60	-	3
b4	Corner contact width, “preferred” option	0.45	-	0.50	3

Notes:
1. Minimum acceptable option to be used when routing prevents preferred or intermediate width contact.
2. Intermediate option to be used when routing prevents preferred width contact.
3. Preferred option to be used when possible.

5. USE OF EE1004-v IN EE1002(A) APPLICATIONS OR TSE2004av IN TSE2002av APPLICATIONS

The interface to the EE/TSE devices are a superset of the feature set of the legacy EE1002(A) and TSE2002av devices with the following exceptions:

- The default EE page address (0) should not be changed if compatibility is required; only 256 bytes are used
- Permanent Write Protect is not supported
- TSE2004av only: TS Capabilities Register values are:
  - Bit 7: EVENT_n capability is only supported with deassertion semantics
  - Bit 6: Wide range bus timeout is not supported
  - Bit 5: VHV is supported by all TSE2004av devices
  - Bit 2: Temperatures below 0 °C are indicated using two's complement values
  - Bit 1: The temperature monitor has ±1 °C accuracy over the active range (75 °C to 95 °C) and 2°C accuracy over the monitoring range (40 °C to 125 °C)
  - Bit 0: Interrupt functionality is supported

6. PROGRAMMING THE EE/TSE

The situations in which the EE/TSE is programmed can be considered under two headings:

- when the DIMM is isolated (not inserted on the PCB motherboard)
- when the DIMM is inserted on the PCB motherboard

6.1. DIMM Isolated

With specific programming equipment, it is possible to define the EE/TSE content, using Byte and Page Write instructions, and its write-protection using the SWPn and CWP instructions. To issue the SWPn and CWP instructions, the DIMM must be inserted in the application-specific slot where the SA0 signal can be driven to V_{HV} during the whole instruction. This programming step is mainly intended for use by DIMM makers, whose end application manufacturers will want to clear this write-protection with the CWP on their own specific programming equipment, to modify the protected bytes, and finally to set the write-protection with the SWPn instruction.

In DIMM Isolation usage, the Read Protection Status (RPSn), Set EE Page Address (SPAn), and Read EE Page Address (RPA) commands are fully supported.

7. PACKAGING

PSON-8. 8-lead plastic small outline no lead package outline (MO-229; 2x3 mm = variation V/WCED-3)

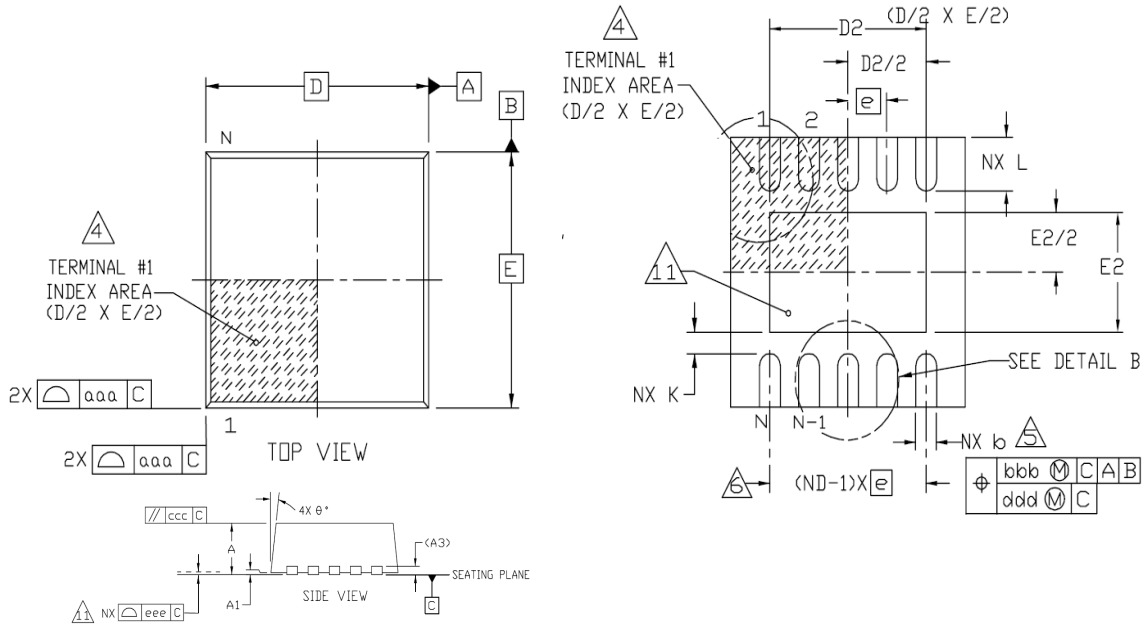
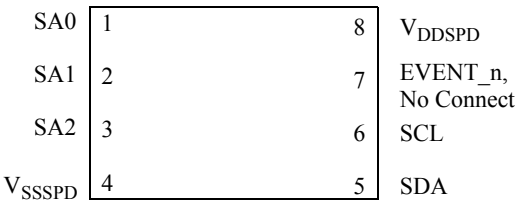


Figure 19 — PSON-8 Package Outline

Table 28 — PSON-8 Critical Package Dimensions

Symbol	Min	Typ	Max	Units	Notes
A	0.80	0.90	1.00	mm	Var. V
A	0.70	0.75	0.80	mm	Var. W
D	--	2.00	--	mm	Basic, Var. V/ WCED-3
D2	1.20	--	1.60	mm	
E	--	3.00	--	mm	Basic
E2	1.20	--	1.60	mm	
L	0.30	--	0.45	mm	
K	0.20	--	--	mm	
N	8			Leads	

Note: Variation V2030D-3 was previously identified as VCED-3, W2030D-3 as WCED-3.

Variation U2030D was not previously identified.

Device Pinout