

PowerVR SGX Series5XT IP Core Family



The PowerVR™ SGX Series5XT Graphics Processing Unit (GPU) IP core family is a series of highly efficient graphics acceleration IP cores that meet the multimedia requirements of the next generation of consumer, communications and computing applications.

PowerVR SGX Series5XT architecture is fully scalable for a wide range of area and performance requirements, enabling it to target markets from low cost feature-rich mobile multimedia products to very high performance consoles and computing devices.

The family incorporates the second-generation Universal Scalable Shader Engine (USSE2™), with a feature set that exceeds the requirements of OpenGL 2.0 and Microsoft Shader Model 3, enabling 2D, 3D and general purpose (GP-GPU) processing in a single core.

Features

- Most comprehensive IP core family and roadmap in the industry
- USSE2 delivers twice the peak floating point and instruction throughput of Series5 USSE
- YUV and colour space accelerators for improved performance
- Upgraded PowerVR Series5XT shader-driven tile-based deferred rendering (TBDR) architecture
- Multi-processor options enable scalability to higher performance
- Support for all industry standard mobile and desktop graphics APIs and operating systems
- Fully backwards compatible with PowerVR MBX and SGX Series5

Benefits

- Extensive product line supports all area/performance requirements
- Low-risk solution for all embedded graphics applications
- Shader-based architecture enables near photo realistic image quality
- Fully compliant proven implementations of all APIs
- Lowest power consumption and silicon footprint
- Low host CPU and memory system bandwidth load

Applications

- Smart and feature phones
- Mobile internet devices (MIDs)
- Personal media players
- Games consoles
- HDTV and set-top boxes
- Personal navigation devices
- In-car navigation and information
- Electronic dashboards
- UMPCs, laptops and netbooks

PowerVR SGX Family

Series5XT	SGX543MP1-16, SGX544MP1-16, SGX554MP1-16
Series5	SGX520, SGX530, SGX531, SGX535, SGX540, SGX545

Multi-standard API and OS Support

Embedded APIs	OpenGL ES 2.0 and OpenGL ES 1.1 + Extension Pack Desktop OpenGL 2.0 (SGX535/545) and 3.0 (SGX545) OpenVG 1.1 enabling Flash and SVG PVR2D for legacy 2D Support (BLTs, ROP2/3/4) OpenWF enabling advanced compositing OpenCL Embedded and Full Profile (SGX545) for GP-GPU
Windows APIs	DirectX9 (SGX535/545) and 10.1 (SGX545)
OS Support	Linux, Symbian and Android Microsoft WinCE and Windows Desktop RTOS on request

Comprehensive Roadmap

PowerVR SGX Series5XT cores extend the SGX family to cover even the highest-end performance/area options, so that the optimal solution is available for every set of application requirements.

Programmable USSE2

USSE2 is a scalable multi-threaded multimedia processing engine offering up to 2x the floating point throughput of earlier Series5 SGX IP cores. An extended instruction set with comprehensive vector operations and co-issue capabilities enables advanced geometry and pixel processing as well as GP-GPU tasks. These tasks are broken down into processing packets which are then scheduled across a number of multi-threaded execution units in the USSE2. This enables optimal hardware load balancing, maximum latency tolerance and efficient gate use, all accessed through a single software programming model and compiler. For maximum efficiency, additional optimized hardware engines, including texture, pixel and tiling accelerators work with USSE2 in the PowerVR SGX Series5XT architecture to deliver even higher anti-aliasing performance. USSE2 enables up to IEEE 754 single precision floating point data processing – essential for the best possible image quality and vital for effective GP-GPU multimedia processing. An advanced microkernel based approach to scheduling ensures maximum performance with minimal CPU load and enables extremely rapid context switching and concurrent multi-API support.

YUV, Colour Space Accelerators and S3D Support

The USSE2 workload is reduced by the addition of dedicated YUV and Colour Space Accelerators for optimal interaction with video cores (e.g., PowerVR VXD). Additionally all SGX cores offer immersive support for Stereoscopic 3D (S3D) display enabling all standard modes with minimal overhead.

Series5XT Shader-driven TBDR Architecture

Unique, patented tiling technology enables on-chip processing of hidden surface removal (pixel perfect and submission order independent) at double the rate of PowerVR Series5. Unlike early Z hierarchical systems used by competing solutions PowerVR offers high performance hidden surface removal irrespective of submission order or primitive orientation resulting in the highest performance hidden surface removal and stencil operation in the industry. The family further extends the bandwidth and power efficiency and performance of hardware-based perfect tiling and culling algorithms, which used in

combination with seamless scene complexity management and compression, enable PowerVR SGX to handle arbitrarily complex scenes in limited memory footprints with the lowest memory bandwidth usage.

Multi-processor Support

Members of the PowerVR SGX Series5XT family offer Multi-Processor (MP) support for 2 to 16 cores (SGX543, SGX544 and SGX554), enabling complete linear scaling of all GPU performance components (Vertex, Pixel, Setup and GP-GPU) with virtually no overhead in bandwidth usage.

Low Power

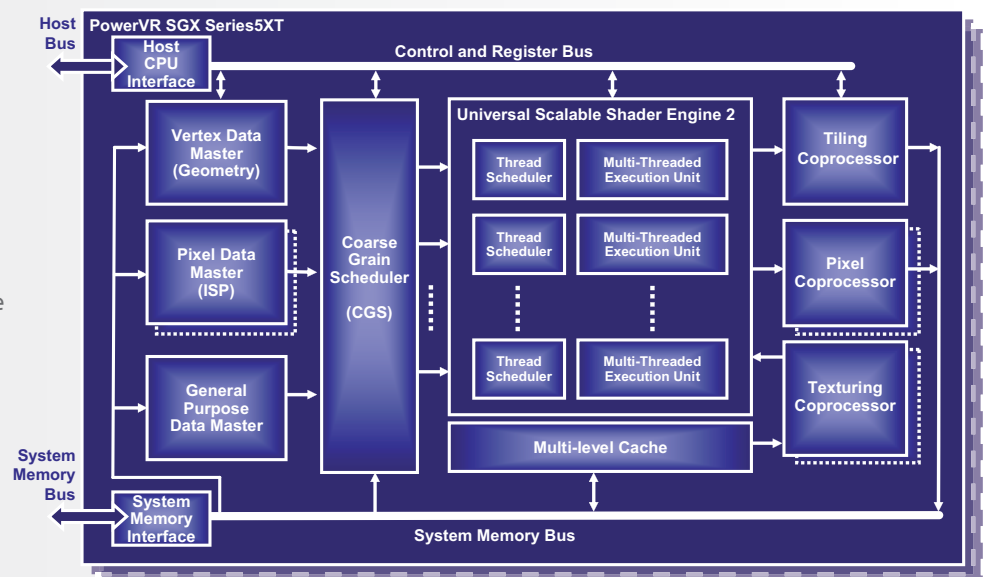
PowerVR SGX Series5XT cores are built on a foundation of unique patented technologies that deliver class leading performance while keeping power dissipation to a minimum. PowerVR's inherently low-power architecture is complemented by the use of the latest sophisticated clock gating techniques to ensure the lowest active and standby power consumption.

High Performance per mW

PowerVR SGX Series5XT core architecture currently comprises SGX543, SGX544 and SGX554 and their respective MP variants covering a wide range of area, feature and performance requirements to accommodate the needs of many target markets. Performance scales with clock speeds from 100 MHz to 400 MHz and beyond.

System Level Cache Option

A range of pre-verified system level cache configurations (32, 64 and 128KB) are available to further reduce bandwidth usage and maximize latency tolerance through access profile optimized caching.



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