HBM Gen2 PHY

Designed for performance and power efficiency in networking and data center applications

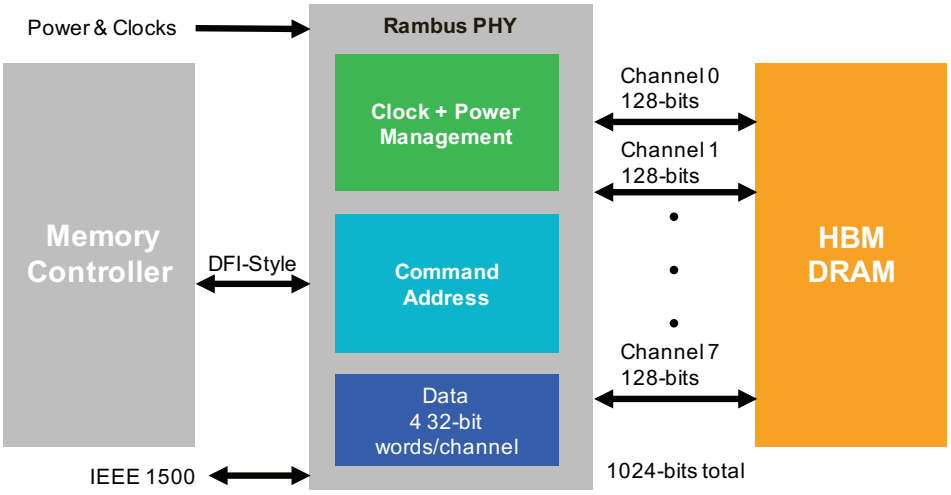
Overview

The Rambus high-bandwidth memory (HBM) PHY is fully compliant to the JEDEC HBM2 standard and is optimized for systems that require a low-latency and high-bandwidth memory solution. The memory subsystem supports data rates up to 2000 Mbps per data pin, resulting in a total bandwidth of 256 GB/s. The interface features 8 independent channels, each containing 128 bits for a total data width of 1024 bits. The PHY is designed for a 2.5D system with a silicon interposer to route signals between the DRAM stack and PHY. Rambus performs complete signal and power integrity analysis on the entire 2.5D system to ensure that all signal, power and thermal requirements are met. By working closely with customers to meet system requirements, Rambus provides design flexibility for a differentiated and easy-to-integrate solution.

The PHY is delivered as a fully characterized hard macro and contains all of the necessary components for robust operation including:

- IO pads
- PLL
- Clock distribution
- Transmit and receive paths
- Control logic
- Power distribution
- Electrostatic discharge (ESD) protection circuitry

HBM PHY Block Diagram



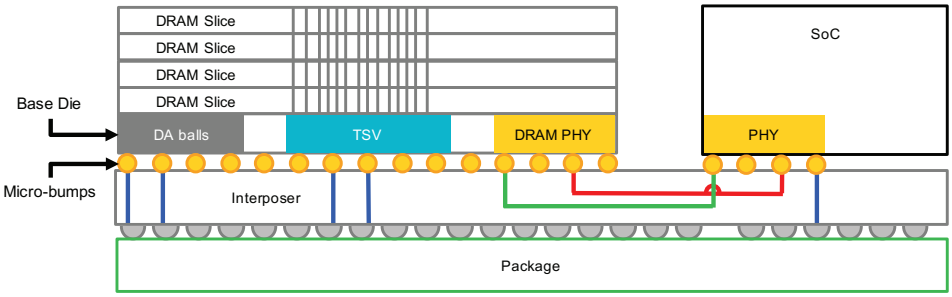
Highlights

- JEDEC HBM2 JESD235A standard compliant
- Advanced process node: 14nm LPP
- 8 channels @ 128 bits/channel
- Up to 2000 Mbps/pin
- Supports DRAM 2, 4, and 8 stack height
- DFI-style interface to Memory controller
- 2.5D interposer connections between PHY and DRAM
- Validated Memory Controller interface
- Support for wafer-level and interposer testing
- Available with LabStation™ Validation Platform for enhanced bring-up and validation

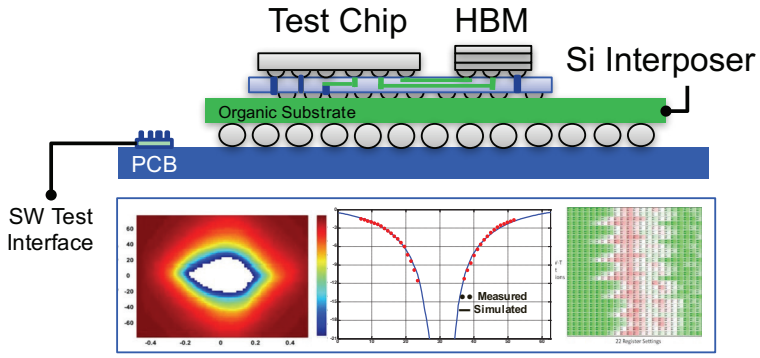
Standards Compatibility

Standards	Data Rates (Gbps)
HBM2	0.5-2000

HBM 2.5D Memory System



Test Chip Environment



Deliverables

Fully-characterized hard macro (GDSII)

Complete design views:

- Gate-level and IO models
- Verification test benches
- Layout abstracts (.lef)
- Timing models (.lib)

Full documentation:

- Datasheet
- Package and interposer design guidelines
- ASIC/DFT manufacturing guidelines
- Test and characterization user guide
- Verilog models
- CDL netlists (.cdl)
- GDSII layout
- DRC & LVS reports

Optional design integration and bring-up support services

Features

- Flexible delivery of IP core: works with ASIC/SoC layout requirements
- Speed bins: 0.5 Gbps, 1.0 Gbps, 1.5 Gbps, 1.6 Gbps, 1.8 Gbps, 2.0 Gbps
- 8 channels and 16 pseudo-channels
- Support for DRAM 2, 4, or 8, stacks
- DFI 3.1 style interface for easy integration with memory controller
- Memory controller or PHY can be ASIC interface master (PHY independent mode)
- Selectable low-power operating states
- Programmable output impedance
- Pin programmable support for lane repair
- ZQ calibration of output impedance
- IEEE 1500 test support
- Autonomous test support
- SSO noise reduction
- Micro-bump pitch matched to the DRAM pitch
- Utilizes 13-layer metal stack
- East-West orientation (PHY can be placed in corner of die)
- Register interface for state observation
- LabStation™ software environment for system level bring-up, characterization, and validation

rambus.com/memoryphys